



# ALAGAPPA UNIVERSITY

[Accredited with 'A+' Grade by NAAC (CGPA:3.64) in the Third Cycle  
and Graded as Category-I University by MHRD-UGC]

**KARAIKUDI – 630 003**

**DIRECTORATE OF DISTANCE EDUCATION**



## M.Sc. [Physics] 345 13



## LINEAR AND INTEGRATED ELECTRONICS

**I - Semester**



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## **LINEAR AND INTEGRATED ELECTRONICS**

#### **Author**

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# SYLLABI-BOOK MAPPING TABLE

## Linear and Integrated Electronics

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Syllabi	Mapping in Book
<b>BLOCK I: SEMICONDUCTOR AND DIODES</b>	
<b>Unit-1: Semiconductor Physics</b> Introduction to Semiconductor–Intrinsic and Extrinsic Semiconductors–PN Junction.	<b>Unit 1: Semiconductor Physics</b> (Pages 1-15);
<b>Unit-2: Semiconductor Diode</b> Forward and Reverse Bias of Diode–Characteristics of Forward and Reverse Bias of Diode–Zener Diode, its Construction and Characteristics–Zener Diode as Voltage Regulator.	<b>Unit-2: Semiconductor Diode</b> (Pages 16-48);
<b>Unit-3: Special-Purpose Diodes</b> Schottky Diode–Tunnel Diode–LED’s.	<b>Unit-3: Special - Purpose Diodes</b> (Pages 49-60)
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<b>Unit-4: Transistors</b> Transistor Action–Transistor Connections: CB, CE and CC Configurations.	<b>Unit-4: Transistors</b> (Pages 61-79);
<b>Unit-5: Transistor Amplifier</b> Transistor as an Amplifier: Class A, Class B and Class C Operations and their Field of Application.	<b>Unit-5: Transistor Amplifier</b> (Pages 80-106);
<b>Unit-6: Transistor Biasing</b> Transistor Biasing and Stabilization–Need for Biasing–DC Load Line–Operating Point–Bias Stability–Transistor Biasing Circuits–Fixed Bias Circuit–Base Bias with Emitter Feedback–Base Bias with Collector Feedback–Voltage Divider Bias Circuit.	<b>Unit-6: Transistor Biasing</b> (Pages 107-122);
<b>Unit-7: Transistor Audio Power Amplifier</b> Class B Push Pull Amplifier–Transformer Coupled Audio Power Amplifier.	<b>Unit-7: Transistor Audio Power Amplifier</b> (Pages 23-127)
<b>BLOCK III: OPTO ELECTRONIC DEVICES AND OSCILLATORS</b>	
<b>Unit-8: Field Effect Transistors and Silicon Controlled Rectifier</b> Construction, Working and I/O Characteristics of FET, JFET, MOSFET and SCR.	<b>Unit-8: Field Effect Transistors and Silicon Controlled Rectifier</b> (Pages 128-153);
<b>Unit-9: Power Electronics and OPTO Electronic Devices</b> Construction, Working and I/O Characteristics of DIAC and TRIAC, Solar Cells, Photo Detectors.	<b>Unit-9: Power Electronics and OPTO Electronic Devices</b> (Pages 154-166);
<b>Unit-10: Sinusoidal Oscillators</b> Oscillator: Wien Bridge–RC Phase Shift, Hartley, Colpitt’s Oscillators.	<b>Unit-10: Sinusoidal Oscillators</b> (Pages 167-187)
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<b>Unit-12: Electrical Parameters of OP-AMP</b> Electrical Parameters–Input Offset Voltage and Current Input Bias Current–Differential Input Resistance–Input Capacitance–Output Offset Voltage and Nullification–CMRR–Slew Rate.	<b>Unit-12: Electrical Parameters of OP-AMP</b> (Pages 199-207);



**Unit-13: Applications of OP-AMP**

Applications of OP-AMP 741: Inverting, Non-Inverting Amplifiers–Adder –Subtractor–Comparator–Differentiator–Integrator–Analog Computation.

**Unit-14: Active Filters**

Active Filters: First Order High Pass and Low Pass Filters, Band Pass Filter.

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**Unit-13:** Applications of OP-AMO

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## INTRODUCTION

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Electronics deals with electrical circuits that involve active electrical components, such as vacuum tubes, transistors, diodes, integrated circuits, optoelectronics, and sensors, associated passive electrical components, and interconnection technologies. Commonly, electronic devices contain circuitry consisting primarily or exclusively of active semiconductors supplemented with passive elements; such a circuit is described as an electronic circuit.

A linear circuit is one that has no nonlinear electronic components in it. Examples of linear circuits are amplifiers, differentiators, and integrators, linear electronic filters, or any circuit composed exclusively of ideal resistors, capacitors, inductors, op-amps (in the ‘non-saturated’ region), and other ‘linear’ circuit elements. An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small flat piece (or ‘chip’) of semiconductor material, normally silicon. The integration of large numbers of tiny transistors into a small chip results in circuits that are orders of magnitude smaller, cheaper, and faster than those constructed of discrete electronic components.

Electronics is now so pervasive that it’s almost easier to think of things that do not use it than of things that do. Entertainment was one of the first areas to benefit, with radio and later television both critically dependent on the arrival of electronic components. Electronic equipment saves our lives in other ways too. Hospitals are packed with all kinds of electronic gadgets, from heart-rate monitors and ultrasound scanners to complex brain scanners and X-ray machines.

This book, *Linear and Integrated Electronics*, is divided into four blocks, which are further subdivided into fourteen units. The first unit introduces the concept of semiconductors while semiconductor diodes have been discussed in the following unit. The third unit deals with special purpose diodes. Transistors are focused on in the fourth unit while the fifth unit explains transistor amplifiers. Transistor biasing is discussed in the sixth unit while seventh unit deals with transistor audio power amplifier. Eighth unit discusses field effect transistors. And power electronics has been explained in the following unit. Sinusoidal oscillators have been explained in the tenth unit while eleventh unit introduces OP-AMP. Twelfth unit discusses electrical parameters of OP-AMP while thirteenth unit explains applications of OP-AMP. The last unit discusses active filters.

The book follows the self-instructional mode wherein each unit begins with an ‘Introduction’ to the topic. The ‘Objectives’ are then outlined before going on to the presentation of the detailed content in a simple and structured format. ‘Check Your Progress’ questions are provided at regular intervals to test the student’s understanding of the subject. ‘Answers to Check Your progress question’, a ‘Summary’, a list of ‘Key Words’ and a set of ‘Self-Assessment Questions and Exercises’ are provided at the end of each unit for effective recapitulation.

## NOTES

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**BLOCK - I**  
**SEMICONDUCTOR AND DIODES**

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*Semiconductor Physics*

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**UNIT 1 SEMICONDUCTOR  
PHYSICS**

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**NOTES**

**Structure**

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**1.0 INTRODUCTION**

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Based on the type of materials, the conductivity of electricity is determined by their atomic structure. There are materials that are good conductors of electricity and insulators of electricity. Insulators are bad conductors of electricity. Materials such as copper, aluminum, brass etc. are a good conductor of electricity. Materials such as rubber, wood, glass etc. are insulators of electricity. The conductivity of the material will be established and understood, if the properties of the materials and their atom structure are analyzed better. In this unit, different types of materials, their atomic structure relevant to the working of the device will be covered. Formation of diodes, characteristics of the diode and the applications of the diode will be covered in this unit.

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**1.1 OBJECTIVES**

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After going through this unit, you will be able to:

- Describe materials
- Understand the concept of semiconductor
- Know about intrinsic and extrinsic semiconductors
- Discuss *p-n* Junction

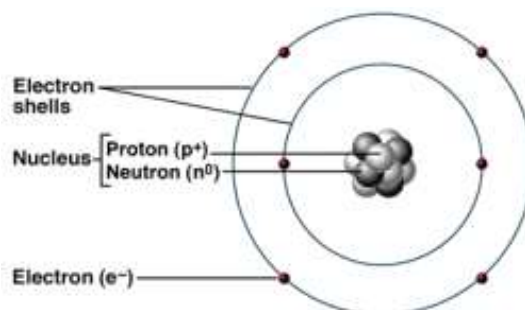


## 1.2 CLASSIFICATION OF MATERIALS

### NOTES

Materials are classified based on the free electrons in the atomic structure. In general, matter includes solids, liquids, and gases. Matter consists of protons, neutrons, and electrons. Protons are positively charged, neutrons are neutral charges and electrons are negatively charged. Protons and neutrons constitute the nucleus of the matter. Electrons revolve around the nucleus in different orbits. The conductivity of the materials depends on the number of free electrons in the outermost of the orbits of the materials.

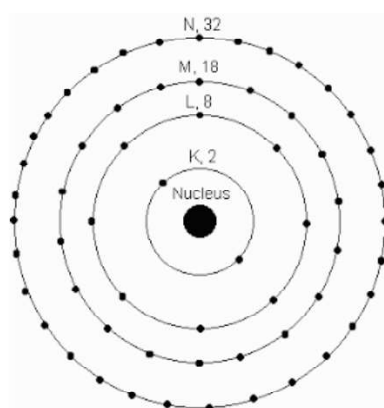
An example of an atomic structure with electrons, protons, and neutrons are given in Figure 1.1. The nucleus that holds the protons and neutrons in the center of the atomic structure determines the number of the electrons revolving around it. The number of electrons and number of protons for a material will be equal in an atomic structure. This neutrality between the protons and electrons make the atoms stable. The number of protons in an atom determines the atomic number of the atom. For example, hydrogen has one proton and one electron and has an atomic number of 1.



**Fig. 1.1** Atomic Structure

The electrons surround the nucleus in different orbits or shells and each shell is attracted towards the nucleus based on the energy level of the orbit. The number of electrons that each shell accommodates is given by, where  $n$  = number of orbits/shell. The shells are designated with alphabets such as K, L, M, N etc.

$n$ / Shell Number	Number of Electrons
1 – K <sup>th</sup> shell	$2 \times 1^2 = 2$ electrons
2 – L <sup>th</sup> shell	$2 \times 2^2 = 8$ electrons
3 – M <sup>th</sup> shell	$2 \times 3^2 = 18$ electrons
4 – N <sup>th</sup> shell	$2 \times 4^2 = 32$ electrons and so on.



**Fig. 1.2** Atomic Structure with Shells

The shells that are closer to the farthest orbit has the least force of attraction with the nucleus. The electrons that are in the  $K^{\text{th}}$  shell of the atom are attracted towards the nucleus stronger such that the energy required to remove them from the shell is equivalent to destroying the atom as a whole. The electrons that are in the outermost orbit has the lesser force of attraction and can be easily removed from the revolving orbit of an atom with less external energy. External energy may be either rise in temperature or by applying an external force such as external potential difference. The electrons that are in the outermost shell are called as **valence electrons**. The outermost orbit may either be completely filled or partially filled. That is, if the outermost orbit can hold 32 number of electrons and if the actual number of electrons in the orbit may be equal to less than 32. If the shells have completely filled electrons, then such atoms are isolated, independent atoms that do not chemically react or bond with other atoms. If the outermost shells have fewer atoms, when such atoms are mixed with other atoms, other atom electrons may bond with the atom to fill the vacant electron spaces in the valence orbit, so that the combined chemical mixture forms a stable mixture.

In general, based on the conductivity of the materials, they are classified as

- Conductors
- Insulators
- Semiconductors

**Conductors** are materials that are very good conductors of electricity and has more free electrons in the valence shell. Such electrons are highly mobile and with a slight external force such as heat or voltage, these electrons are liberated from their orbital revolutions and are free to move thus constituting the electricity.

**Insulators** are materials that are very bad conductors of electricity. The valence electrons in the outermost orbits are bonded tightly to their nucleus and are very difficult to dislocate from their orbital shells. Such materials do not contribute and free electrons and hence the conductivity are very less making them bad conductors of electricity.

## NOTES

## NOTES

Semiconductors are materials that have neither the property of the conductor nor the property of insulator. They are normally insulators, but under certain property changes, they become conductors. Such materials have few valence electrons in their outermost shells which can be delocated by applying external forces.

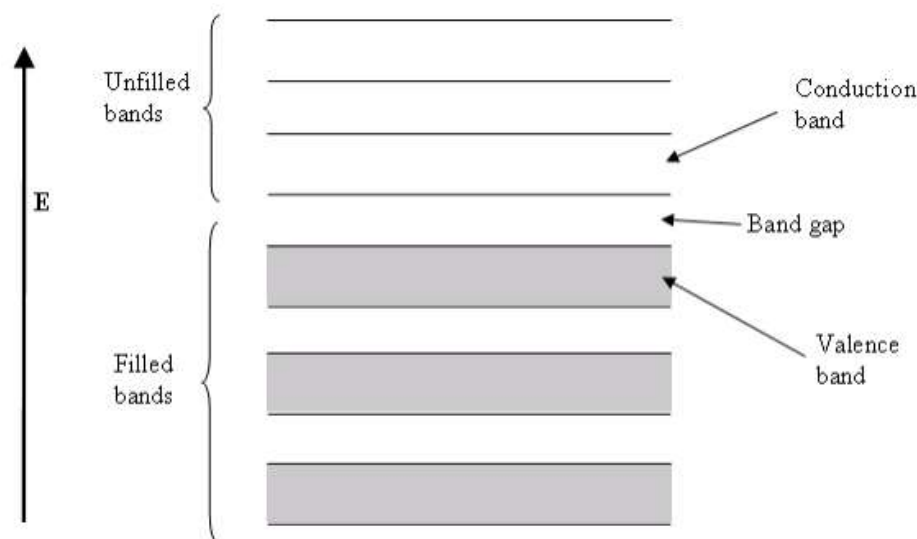
**Energy band theory**

As discussed earlier regarding the energy levels of the nucleus and their force of attraction towards the electron shells, the same can be described using bands of energy associated with nucleus and electron shells with the help of **energy band diagram**.

Energy band diagram consists of three types of the band such as

- Valence band
- Conduction band
- Forbidden band.

The diagram below in Figure 1.3 shows the energy band diagram associated with an atom.



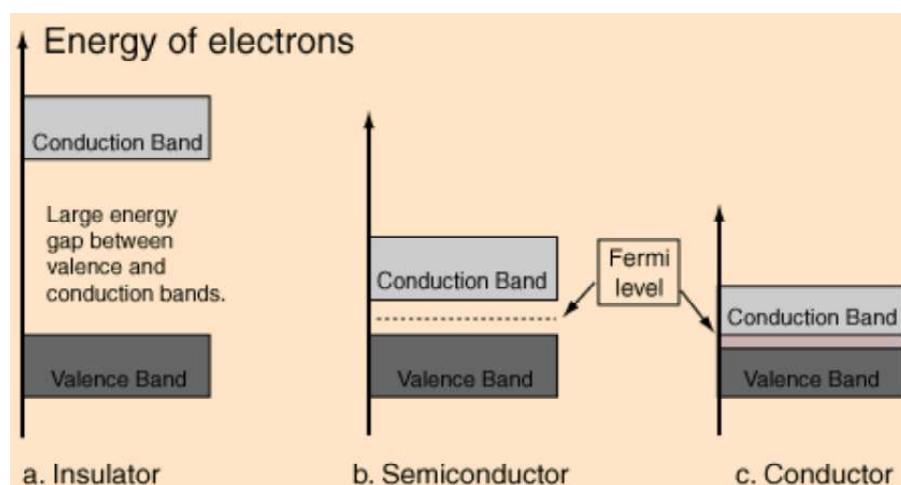
**Fig. 1.3** Energy Band Diagram

The above energy band diagram has the nucleus boundary at the bottom of the band diagram. Each shell has a band of energy. The bonding energy between the shells and the nucleus decreases moving farther away from the nucleus energy level. Hence the valence energy band has the least force attraction from the nucleus. The conduction band in the above Figure 1.3 depicts the energy band in which the electrons are free to move and contribute to the conductivity of the material. The energy gap between the valence band and the conduction band is called as **forbidden energy gap**. Lesser the forbidden energy gap, lesser is the energy required to make the electrons in the valence band to move to the conduction

band, i.e. lesser energy is required to dislocate the valence electrons to make it free electrons contributing to the conduction of electricity. The median energy level between the conduction band and the valence band is known as **Fermi level**.

The energy band diagram of the conductor, insulator, and semiconductors are given in Figure 1.4. In conductors, the valence band and conduction band overlap each other. Under normal room temperature, the conductors have free electrons moving between the valence band and conduction band. No external energy is required to dislocate the electrons to make it free and conducting. In semiconductors, there exists a forbidden energy gap, . An external energy equivalent to is required to be applied to dislocate electron from valence band to conduction band. In insulators, the forbidden gap between the valence band and the conduction band is larger than the other two materials. The energy required to dislocate the electrons in the valence band to conduction band is sufficient enough to damage the material permanently.

## NOTES



**Fig. 1.4** Energy Band Diagram of Conductor, Semiconductor, and Insulator

### Check Your Progress

1. What are valence electrons?
2. What are semiconductors?
3. What are insulators?

## 1.3 INTRINSIC AND EXTRINSIC SEMICONDUCTORS

This text focuses on the semiconductors and their properties. Most widely used semiconductors are Silicon (Si), Germanium (Ge), Selenium (Se) etc., that exists as simple semiconductors and compound semiconductors such as Gallium Arsenide

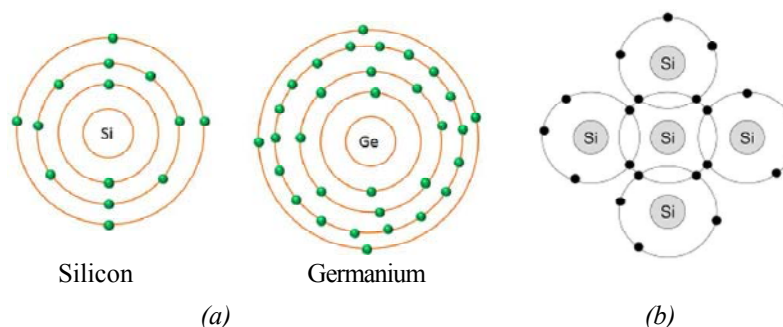
(GaAs), Indium Phosphate (InP), Gallium Nitride (GaN) etc. Semiconductors based on the purity of the materials are classified as

- Intrinsic Semiconductors
- Extrinsic semiconductors

## NOTES

### 1.3.1 Intrinsic Semiconductors

Semiconductors that exist in pure form without any impurities added are called as intrinsic semiconductors. Consider the semiconductor Silicon, Si with atomic number 14. It has 14 number of protons and 14 number of electrons. The first shell occupies 2 electrons, the second shell occupies 8 electrons and the third shell which could accommodate 18 electrons has only 4 valence electrons. Similarly, germanium with an atomic number of 32 as shown in Figure 1.5a has 4 shells with an outermost shell consisting of 4 valence electrons. These atoms exist in the crystalline structure with bonding as shown in Figure 1.5b. One atom of silicon shares the bonding with 4 other atoms thereby filling the 3rd shell of an atom with all 8 electrons creating a stable composition of silicon crystal. This type of bonding is known as covalent bonding.



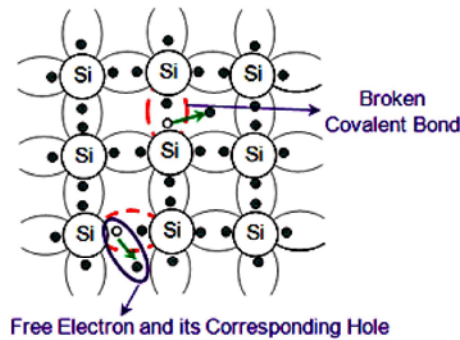
**Fig. 1.5** (a) Atomic Structure of Silicon and Germanium,  
(b) Crystalline Structure of Silicon

Intrinsic semiconductors behave as perfect insulators under normal room temperatures. Silicon and germanium that consists of 4 valence electrons in their outermost shells are also known as **tetravalent atoms**. Similarly, atoms with three valence electrons are known as **trivalent atoms** and atoms with five valence electrons are known as **pentavalent atoms**.

### Conduction in Intrinsic Semiconductors

When an external energy is supplied to the intrinsic semiconductor crystal, the electrons absorb the energy supplied and gain enough energy to break the covalent bond and are set free to move as free electrons in the crystal. Such free electrons move randomly inside the crystal until they lose their energy and find a bonding pair of an electron with some other atom. When the electron leaves a covalent bond due to external energy, they leave behind a vacant space known as holes. Electrons are negatively charged and the vacant hole spaces wanting for electrons

to occupy the space are considered as positively charged. When the free electrons leave the covalent bonding due to external energy, they form an electron-hole pair.

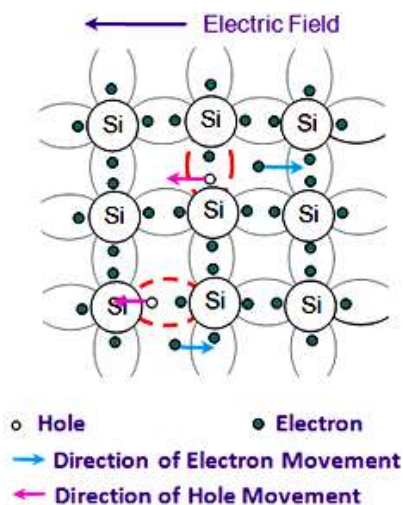


**Fig. 1.6** Conduction Inside Intrinsic Semiconductors

### Electron Current and Hole Current

Current constituted by electrons inside the semiconductor crystal are called an **electron current**. Since electrons are negatively charged, when a potential is applied across the semiconductor crystal, the electrons are attracted towards the positive terminal of the battery.

Current constituted by holes inside a semiconductor crystal are known as **hole current**. Though the holes (vacant spaces) do not move, consequent movement of electrons creates an illusion such that holes move, but in the opposite direction as that of the electron. Electron movement occurs towards the positive polarity of the battery and the hole movement is illusioned to appear as though holes move towards negative terminal of the battery. The movement of holes, i.e., the movement towards a negative terminal (from the positive terminal) is considered as the conventional current movement and hence the hole movement is considered as conventional current flow and the electron movement is considered as the electron flow. The electron and hole current is depicted in Figure 1.7



**Fig. 1.7** Electron and Hole Current

### NOTES

**NOTES**

The hole current is known as the conventional current is opposite to the direction of the electron movement and flows from the positive terminal of the battery to the negative terminal of the battery. The electron current and hole current occur due to two process, they are

- Drift and
- Diffusion.

**Drift Current**

The current flow that takes place due to the application of the external potential through a battery results in drifting of the electrons, thereby resulting in drift current. When an external energy is applied to the semiconductor crystal, the electrons gain energy and starts to drift across the crystal and tends move towards the battery terminal (positive terminal). Such currents are said to be drift current caused due to drifting of electrons.

**Diffusion Current**

Diffusion current occurs due to the movement of electrons through diffusion when they move from higher concentration area to a lower concentration area of the semiconductor crystal without applying any external force or energy.

**1.3.2 Extrinsic Semiconductors**

An extrinsic semiconductor is one that has been doped, i.e., during manufacture of the semiconductor crystal a trace element or chemical called a doping agent has been incorporated chemically into the crystal, for the purpose of giving it different electrical properties than the pure semiconductor crystal, which is called an intrinsic semiconductor. In an extrinsic semiconductor, these foreign dopant atoms in the crystal lattice provide the charge carriers which carry electric current through the crystal. The doping agents used are of two types, resulting in two types of extrinsic semiconductor. An electron donor dopant is an atom which, when incorporated in the crystal, releases a mobile conduction electron into the crystal lattice. An extrinsic semiconductor which has been doped with electron donor atoms is called an *n*-type semiconductor, because the majority of charge carriers in the crystal are negative electrons. An electron acceptor dopant is an atom which accepts an electron from the lattice, creating a vacancy where an electron should be called a hole which can move through the crystal like a positively charged particle. An extrinsic semiconductor which has been doped with electron acceptor atoms is called a *p*-type semiconductor, because the majority of charge carriers in the crystal are positive holes.

Doping is the key to the extraordinarily wide range of electrical behaviour that semiconductors can exhibit, and extrinsic semiconductors are specifically used to make semiconductor electronic devices, such as diodes, transistors, integrated circuits, semiconductor lasers, LEDs, and photovoltaic cells. Sophisticated

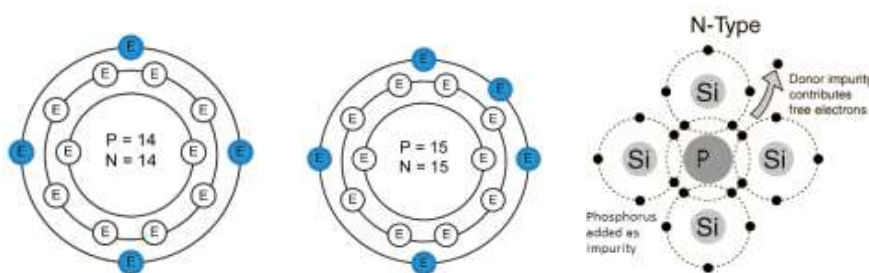
semiconductor fabrication processes like photolithography can implant different dopant elements in different regions of the same semiconductor crystal wafer, creating semiconductor devices on the wafer's surface. For example a common type of transistor, the  $n$ - $p$ - $n$  bipolar transistor, consists of an extrinsic semiconductor crystal with two regions of  $n$ -type semiconductor, separated by a region of  $p$ -type semiconductor with metal contacts attached to each part.

Intrinsic semiconductors are the purest form of semiconductors. Their conductivity of electricity is limited. They have an equal number of electrons and holes. To make semiconductors practically relevant with better conduction of current, it is important to enhance the conduction capability of semiconductors. One such technique to enhance the conductivity is by the process of **doping**. Doping is a process of adding impurities to the intrinsic semiconductors, such that the conductivity of the semiconductors is improved. The impurity that is added to the semiconductor is called as a dopant. The doped semiconductors are called as extrinsic semiconductors. The type of impurities added may enhance the number of electrons or they may enhance the number of holes. Hence, depending on the type of impurities, the extrinsic semiconductors can be classified as

- $n$ -type semiconductors
- $p$ -type semiconductors.

When an intrinsic semiconductor is added with an impurity with pentavalent atoms,  $n$ -type semiconductors are formed. When an intrinsic semiconductor is added with a trivalent impurity atom,  $p$ -type semiconductors are formed. Pentavalent impurity atoms are also known as donor atoms and trivalent atoms are known as acceptor atoms. Atoms that donate atoms to the host atoms are called donor atoms and the atoms that accept an electron from the host atoms are called acceptor atoms.

### $n$ -Type Semiconductor



**Fig. 1.8**  $n$ -Type Semiconductor

When a pentavalent impurity atom from group V of the periodic table such as Phosphorus (P) or Arsenic (As) is added to the intrinsic silicon atom,  $n$ -type semiconductors are formed.

When the  $n$ -type impurity atom (donor atoms) is added with the intrinsic silicon atom, the four valence electrons out of five valence electrons in the impurity

## NOTES

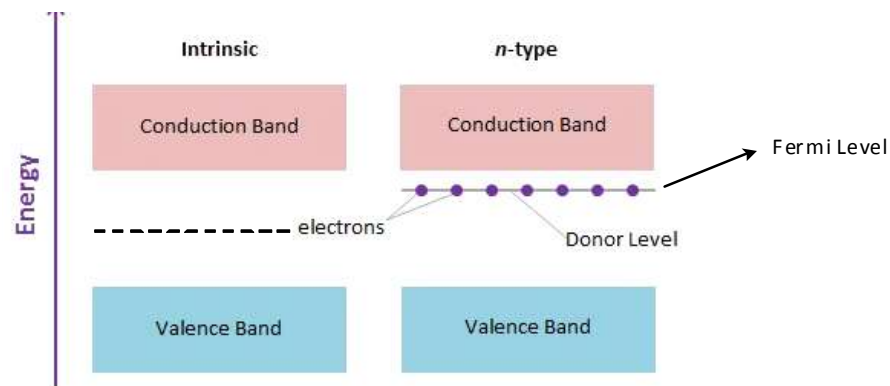


## NOTES

atom forms a covalent bond with the four silicon atoms as shown in Figure 1.8. The remaining one valence electrons from the impurity atoms remain as free electron inside the mixture crystal. Similarly, when 1 of phosphorus can generated free electrons of the order of number of free electrons. Number of free electrons required are controlled by the amount of pentavalent impurity added to the intrinsic silicon atom.

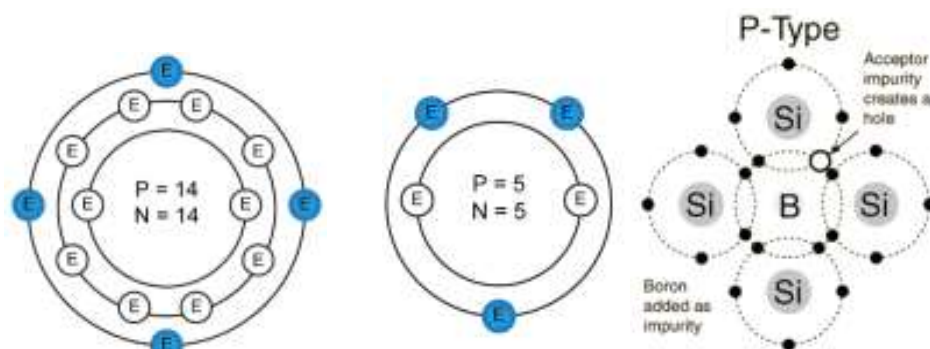
### The conductivity of *n*-type semiconductors

The mobility of electrons is approximately three times that of the mobility of holes. When more free electrons are added to the intrinsic semiconductor, the average energy level of the semiconductor increases. This makes the electrons move easier from the valence band to the conduction band even with an application of the small amount of an external potential. In addition, the Fermi level, which marks the energy level of electrons is closer to the conduction band as shown in Figure 1.9. In *n*-type semiconductors since the electrons are more than the number of holes, electrons are known as majority carriers and the holes are known as minority carriers. The current constituted by majority carriers (electrons) are predominant and the current constituted by minority carriers (holes) are negligible.



**Fig. 1.9** *n*-Type Semiconductor Band Diagram

### *p*-Type Semiconductors



**Fig. 1.10** *p*-Type Semiconductor

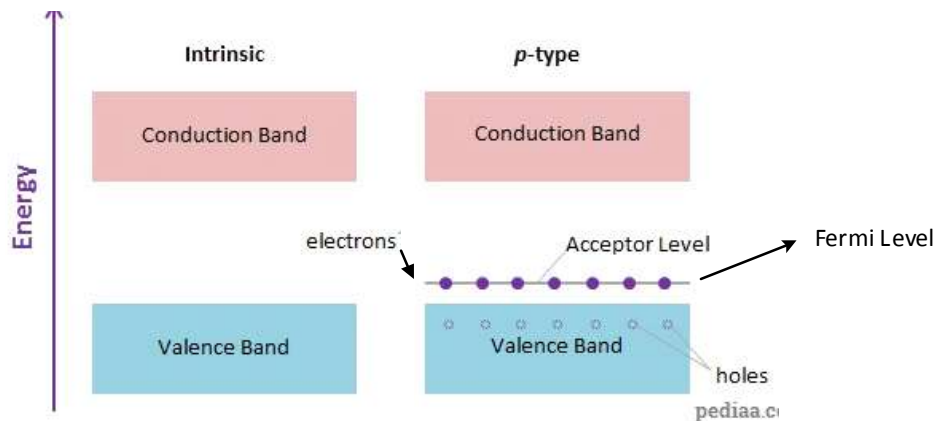
When a trivalent impurity atom from group III of the periodic table such as Boron (B) or Gallium (Ga) is added to the intrinsic silicon atom,  $p$ -type semiconductors are formed.

When the  $p$ -type impurity atom (acceptor atoms) is added with the intrinsic silicon atom, the three valence electrons of the acceptor atoms form a covalent bond with the three silicon atoms leaving behind one silicon atom form an electron-hole pair as shown in Figure 1.10. The one hole generated due to nonavailability of an electron to fill from the impurity atom forms one electron-hole pair. Similarly, when 1 of Boron can generated electron-hole pairs of the order of number of holes. Number of holes required are controlled by the amount of trivalent impurity added to the intrinsic silicon atom.

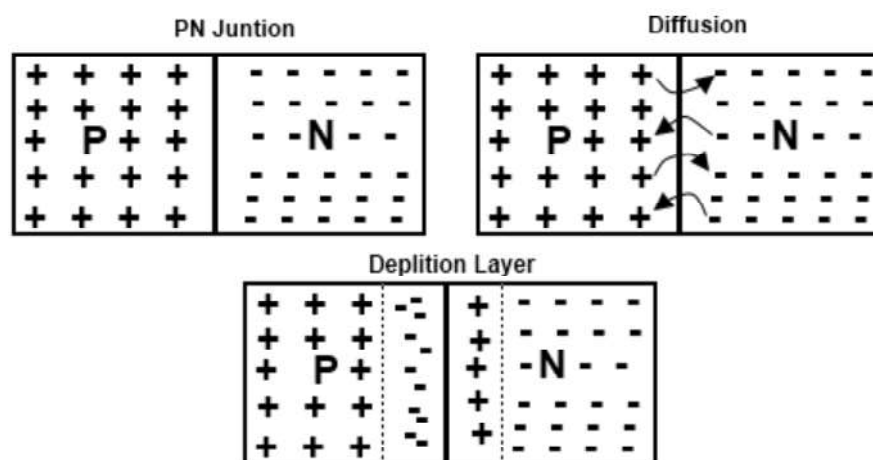
## NOTES

### The conductivity of $p$ -type semiconductors

When more holes are added to the intrinsic semiconductor, the average energy level of the semiconductor decreases. Hence, a larger magnitude of external energy needs to be applied to make the electrons conduct. In other words to make the electrons move from the valence band to conduction band. However, it is easier to make the electrons conduct in the reverse direction by applying a negative potential. The Fermi level, which marks the energy level of electrons is closer to the valence band as shown in Figure 1.11. In  $p$ -type semiconductors since the holes are more than the number of electrons, holes are known as majority carriers in  $p$ -type semiconductors and the electrons are known as minority carriers. The current constituted by majority carriers (holes) are predominant and the current constituted by minority carriers (electrons) are negligent.



**Fig. 1.11**  $p$ -Type Semiconductor Band Diagram

**NOTES****Fig. 1.12** *p-n Diffusion*

When a *p*-type semiconductor and *n*-type semiconductor are joined together, diffusion takes place. Since the *p*-type material is highly concentrated with holes leading to an overall high positive charge material and *n*-type a negatively charged material due to the concentration of electrons, when joined together, they together generate a high potential on the *p*-type side and now potential on the *n*-type side. This leads to the process of diffusion making the electrons to move towards the *p*-side. As electrons move towards the *p*-type crossing the junction, they leave behind holes. The electrons spend enough energy to cross over the junction after which they occupy a hole position nearer to the junction. Thus, holes are formed on the *n*-type side of the junction and electrons on the *p*-type junction. Any electron that wants to cross over the junction further must have enough energy to overcome the holes and the junction together. Thus, creates a region of depletion of charges with positive charges on *n*-type and negative charges on *p*-type. The buildup of the depletion region continues until the electrons cannot diffuse further. Once the diffusion stops, the potential difference created by the process of electron diffusion results in approximately 0.7 volts for silicon semiconductors and 0.3 volts for germanium semiconductors. This potential difference created by the process of diffusion is also known as barrier potential. The electrons that require moving to the *p*-type material further must overcome the barrier potential of 0.7V for silicon material. The electrons alone do not possess such amount of energy to cross the barrier potential and hence on the application of an external voltage equal to the barrier potential is required to make the electrons move to the other side of the *p-n* junction.

The barrier potential depends on various factors as follows:

- Type of semiconductor
- Type of impurity

- External atmospheric temperature and
- The concentration of intrinsic semiconductor

### Check Your Progress

4. What are intrinsic semiconductors?
5. What are extrinsic semiconductors?
6. What is doping?
7. What are the factors on which barrier potential depend?

### NOTES

## 1.4 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

1. The electrons that are in the outermost shell are called as valence electrons.
2. Conductors are materials that are very good conductors of electricity and has more free electrons in the valence shell.
3. Insulators are materials that are very bad conductors of electricity. The valence electrons in the outermost orbits are bonded tightly to their nucleus and are very difficult to dislocate from their orbital shells.
4. Semiconductors that exists in pure form without any impurities added are called as intrinsic semiconductors.
5. An extrinsic semiconductor is one that has been doped, i.e., during manufacture of the semiconductor.
6. Doping is a process of adding impurities to the intrinsic semiconductors, such that the conductivity of the semiconductors is improved. The impurity that is added to the semiconductor is called as a dopant.
7. Type of semiconductor, type of impurity, external atmospheric temperature and the concentration of intrinsic semiconductor.

## 1.5 SUMMARY

- Materials are classified based on the free electrons in the atomic structure. In general, matter includes solids, liquids, and gases.
- Matter consists of protons, neutrons, and electrons. Protons are positively charged, neutrons are neutral charges and electrons are negatively charged.
- The number of electrons that each shell accommodates is given by,  $2n^2$ , where  $n$  = number of orbits/shell.
- The shells that are closer to the nucleus are attracted to the nucleus with greater force of attraction and the one with the farthest orbit has the least force of attraction with the nucleus.

**NOTES**

- The electrons that are in the outermost shell are called as valence electrons.
- Conductors are materials that are very good conductors of electricity and has more free electrons in the valence shell.
- Insulators are materials that are very bad conductors of electricity.
- The energy gap between the valence band and the conduction band is called as forbidden energy gap.
- Semiconductors that exists in pure form without any impurities added are called as intrinsic semiconductors
- An extrinsic semiconductor is one that has been doped, i.e., during manufacture of the semiconductor.

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## 1.6 KEY WORDS

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- **Electron:** A stable subatomic particle with a charge of negative electricity, found in all atoms and acting as the primary carrier of electricity in solids.
- **Proton:** A stable subatomic particle occurring in all atomic nuclei, with a positive electric charge equal in magnitude to that of an electron.
- **Neutron:** A subatomic particle of about the same mass as a proton but without an electric charge, present in all atomic nuclei except those of ordinary hydrogen.

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## 1.7 SELF ASSESSMENT QUESTIONS AND EXERCISES

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**Short Answer Questions**

1. Describe the structure of the atom.
2. What do you mean by doping?
3. What are *p*-type semiconductors?
4. What are *n*-type semiconductors?
5. How is *p-n* junction formed?
6. What do you understand by electron-hole pair?

**Long Answer Questions:**

1. Describe briefly Extrinsic and intrinsic semiconductors with neat diagram
2. Explain electron and hole current in semiconductors?
3. Explain the process of formation of *p-n* junction diode.

4. Explain the energy band diagram of  $p$ -type and  $n$ -type?
5. Explain the energy band diagram of conductors, insulators and semiconductors

*Semiconductor Physics*

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## 1.8 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

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## NOTES

## UNIT 2 SEMICONDUCTOR DIODE

### NOTES

#### Structure

- 2.0 Introduction
- 2.1 Objectives
- 2.2  $p$ - $n$  Junction Diode
  - 2.2.1 Forward biased  $p$ - $n$  Junction Diode
  - 2.2.2 Reverse biased  $p$ - $n$  Junction Diode
- 2.3 V-I Characteristics of  $p$ - $n$  Junction Diode
  - 2.3.1 Diode Equation
  - 2.3.2 Comparison of Diode Breakdown Voltage
  - 2.3.3 Diode Equivalent Circuit
  - 2.3.4 Application of Diode
- 2.4 Zener Diode
  - 2.4.1 Zener Diode as a Voltage Regulator
- 2.5 Answers to Check Your Progress Questions
- 2.6 Summary
- 2.7 Key Words
- 2.8 Self Assessment Questions and Exercises
- 2.9 Further Readings

### 2.0 INTRODUCTION

In this unit, you will study about semiconductor diode. A diode made of semiconductor components, usually silicon. The cathode, which is negatively charged and has an excess of electrons, is placed adjacent to the anode, which has an inherently positive charge, carrying an excess of holes. At this junction a depletion region forms, with neither holes nor electrons. A positive voltage at the anode makes the depletion region small, and current flows; a negative voltage at the anode makes the depletion region large, preventing current flow. Further in this unit,  $p$ - $n$  junction diode are discussed in detail. The basic diode  $p$ - $n$  junction is used throughout the whole of the electronics industry today. Even in its basic form as a diode, it is used in enormous quantities, but beyond that the  $p$ - $n$  junction forms the bedrock of much of today's high-tech transistors and integrated circuits. Without the PN junction, life today would be very different, and electronics would be a very different scene.

### 2.1 OBJECTIVES

After going through this unit, you will be able to:

- Know about forward and reverse bias of diode
- Understand characteristics of forward and reverse bias of diode

- Discuss Zener diode and its construction
- Describe Zener diode as voltage regulator

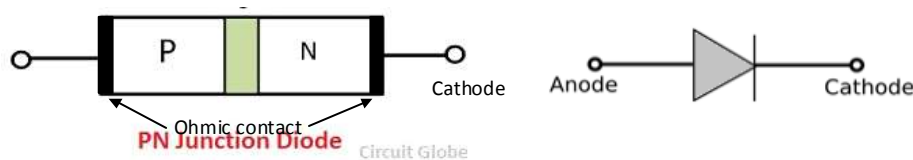
## 2.2 $p$ - $n$ JUNCTION DIODE

### NOTES

The  $p$ - $n$  junction thus formed in the previous section is a popular semiconductor device known as  $p$ - $n$  junction diode. The  $p$ - $n$  junction diode has

- $p$ -type material
- $n$ -type material and
- Depletion layer or barrier potential

The electrode terminals are joined on both the sides of the  $p$ - $n$  junction diode, one on the  $p$ -type side and the other on the  $n$ -type side. The electrode terminals are connected to the  $p$ -type and  $n$ -type materials using metals through an ohmic contact. The schematic diagram of the  $p$ - $n$  junction diode is given in Figure 2.1a and the circuit symbol of  $p$ - $n$  junction diode is given in Figure 2.1b.



**Fig. 2.1** (a)  $p$ - $n$  Diode (b) Circuit Symbol of a  $p$ - $n$  Diode

The terminal connected to  $p$ -type is called anode that represents the positive polarity and the terminal connected to the  $n$ -type is called as cathode representing the negative polarity. The circuit symbol of the diode resembles that of an arrow representing the conventional current direction. The line after the arrowhead of the circuit symbol represents the barrier potential.

### Biased $p$ - $n$ junction diode

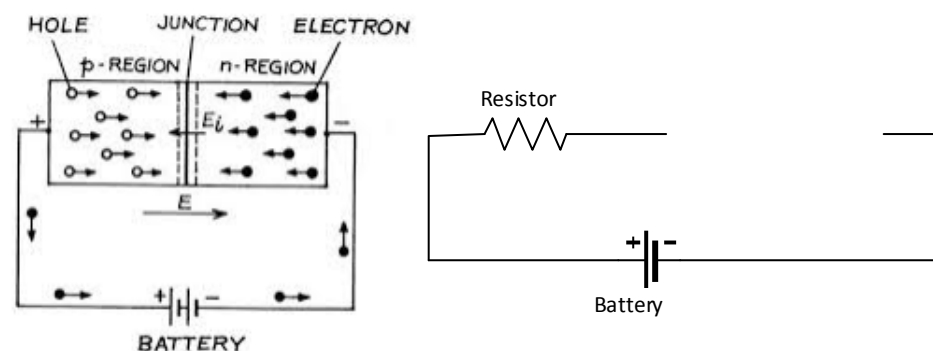
Biasing is the process of applying an external dc voltage to the device such that the device works under the proper operating region. In  $p$ - $n$  junction diode, based on the potential of the battery or an external voltage source applied to the  $p$ -type terminal and  $n$ -type terminal, biasing has been classified as

- Forward biasing
- Reverse biasing



### 2.2.1 Forward biased $p$ - $n$ junction diode

#### NOTES



*Fig. 2.2 Forward Biasing of Diode*

As shown in Figure 2.2, when positive terminal of the battery is connected to anode or  $p$ -type and negative terminal of the battery is connected to the cathode or  $n$ -type material the diode is said to be forward biased.

#### Working of the diode during forward biasing

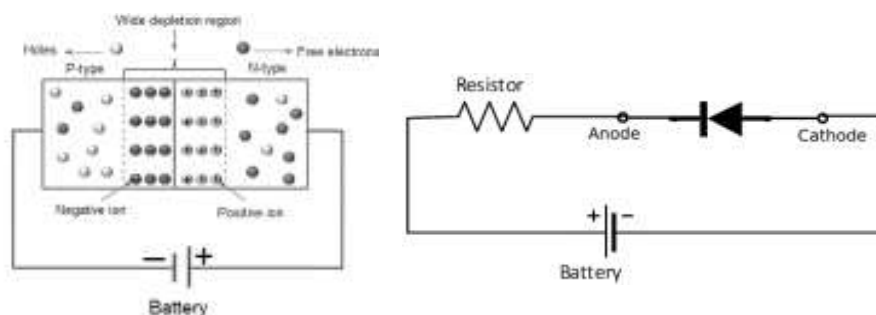
During forward biasing, the positive terminal of the battery is connected to the  $p$ -type material and the negative terminal is connected to the  $n$ -type. The electrons from the negative terminal of the battery are injected into the  $n$ -type material. The injected electrons have enough energy from the battery to cross over the barrier potential when the applied voltage is greater than 0.7 V for a silicon diode. The same time, the minority carriers in the  $p$ -type semiconductor of the diode get attracted towards the positive terminal of the battery and moves towards the positive battery terminal. This leaves behind a large number of holes on the  $p$ -type side. As the electrons start moving from  $n$ -type to  $p$ -type side, it resembles as though the holes move from  $p$ -type side of the diode to the  $n$ -type side of the diode. The movement of an electron from  $n$ -type to  $p$ -type through the barrier potential constitute electron current and conventional current flow (hole current) flows from  $p$ -type to  $n$ -type of the diode. The conventional current is also called as forward current.

#### Effect of depletion region during forward bias

It is to be recalled that, the depletion region has negative potential on the  $p$ -type side (enough electrons on the  $p$ -type side) and a positive potential on the  $n$ -type side (devoid of electrons on the  $n$ -type side). With forward biasing the diode, the electrons flow into the depletion region, thereby reducing the positive ions and increasing the negative ions. This decreases the width of the depletion region.

## 2.2.2 Reverse Biased $p$ - $n$ Junction Diode

Semiconductor Diode



**Fig. 2.3** Reversing Biasing of Diode

During reverse bias, the positive terminal of the battery is connected to the  $n$ -type material and the negative terminal of the battery is connected to the  $p$ -type material. When the  $n$ -type material is connected to positive terminal of the battery, electrons in  $n$ -type material gets attracted towards the positive terminal. On the other side of the battery, the negative terminal of the battery injects more number of electrons into the  $p$ -type side of the diode. This reduces the number of holes in the  $p$ -type side. As the potential of the battery increases further, the electrons that are inside the depletion region are also attracted by the potential of the battery and hence the electrons move towards the positive terminal of the battery creating more number of holes in the depletion region as well. This process widens the depletion region and hence making the electron crossover difficult. The current conduction during reverse bias is majorly due to minority carriers and in the opposite direction. When the potential applied to the diode is much larger, the reverse breakdown of the diode takes place making the minority carriers to move much swifter contributing to the large reverse bias current. This current is known as a reverse breakdown current. On further increasing the reverse bias potential, damages the diode due to an avalanche of electrons known as avalanche breakdown occurs. The electrons gain enough energy to knock down other paired electrons leading to multiplication of electrons.

### Effect of depletion region during reverse bias

During reverse bias, the depletion region width increases due to the removal of a huge number of electrons from the  $p$ -type side and holes from the  $n$ -type side of the depletion region.

#### Check Your Progress

1. What is anode?
2. What is cathode?
3. What is biasing?

## NOTES

## 2.3 V-I CHARACTERISTICS OF $p$ - $n$ JUNCTION DIODE

### NOTES

V-I characteristics of a  $p$ - $n$  junction diode is plotted between the voltage applied across the diode and current flowing through the diode. The magnitude of the current flowing through the diode depends on the voltage applied across the diode. Hence, the voltage is an independent parameter and the current is a dependent parameter. The independent parameter,  $v$  is on the  $x$ -axis and dependent parameter  $i$  is on the  $y$ -axis. The VI characteristics of the diode have two regions, forward bias region and reverse bias region.

When the diode is forward biased, the diode conducts only after the threshold voltage or knee voltage as shown in Figure 2.4.

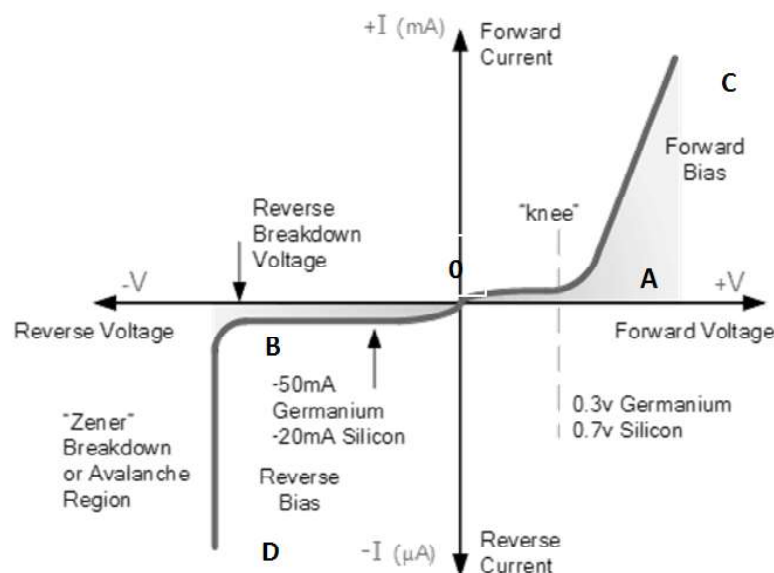


Fig. 2.4  $v$ - $i$  Characteristics of Diode

The knee voltage for silicon-based diodes are around 0.7 volts and for germanium-based diodes are around 0.3 volts.

### The Internal Resistance of the Diode

The  $v$ - $i$  characteristics also provide the internal resistance of the diode. The resistance may be static resistance or dynamic resistance. The slope between  $v$  and  $i$  in the characteristics gives the static resistance.

$$\text{static Resistance, } R = \frac{v}{i} = \text{ohms}$$

$$\text{dynamic resistance, } r = \frac{\Delta v}{\Delta i} \text{ ohms}$$

In the region between O and A of the  $v$ - $i$  characteristics of the diode, the increases slowly till they knee voltage. In this region, the resistance of the diode is very large. In the region between A and C, the current increases drastically very small applied voltage. The resistance calculated in this region is very small, meaning, the diode offers very low resistance allowing huge current to flow across it.

In the reverse bias region of the  $V$   $I$  characteristics of the diode, the diode does not conduct and hence almost 0 current flows through the diode. However, there is a small current that flows inside the diode due to minority carriers in the opposite direction of magnitude approximately in  $\mu A$ . This region is depicted in Figure 2.4 as OB. On further increasing the negative voltage, reverse breakdown occurs and after which the negative current increases drastically. For silicon semiconductors, the reverse breakdown occurs approximately at -20 mA and for germanium semiconductors, reverse breakdown occurs approximately at -50 mA. This reverse breakdown region is also known as Zener breakdown region. This region is known as Zener breakdown because a device known as Zener diode which will be dealt in with further units operate predominantly in this region.

Increasing the negative voltage further beyond the reverse breakdown leads to a multiplication of electrons by avalanche leading to an avalanche breakdown.

### 2.3.1 Diode Equation

The mathematical expression for the diode current as a dependent function on diode voltage, that depicts the  $v$ - $i$  characteristics of the diode is given by

$$I = I_0 \left[ e^{\left( \frac{V}{\eta V_T} \right)} - 1 \right] A$$

where,  $I_0$  = Reverse Saturation current (A)  
 $V$  = Applied diode voltage (V)  
 $V_T$  = Temperature dependent voltage (V)

$$= kT = \frac{T}{11600} \text{ at } 27^\circ\text{C}$$

$\eta = 1$  for Germanium diodes  
 $\eta = 2$  for Silicon diodes

Also,  $k$  = Boltzmann's constant =  $8.62 \times 10^{-5} \text{ eV}^\circ\text{K}$   
 $T$  = Temperature ( $^\circ\text{K}$ )

## NOTES

### 2.3.2 Comparison of Diode Breakdown Voltage

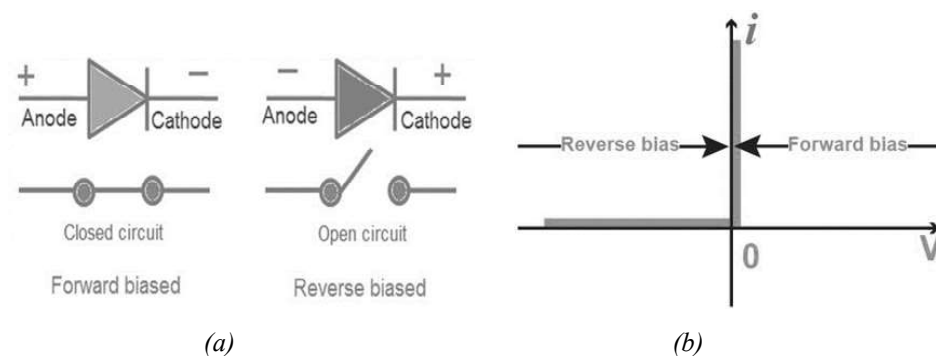
#### NOTES

Basis For Comparison	Avalanche Breakdown	Zener Breakdown
Definition	The avalanche breakdown is a phenomenon of increasing the free electrons or electric current in semiconductor and insulating material by applying the higher voltage.	The process in which the electrons are moving across the barrier from the valence band of the $p$ -type material to the conduction band of the lightly filled $n$ -material is known as the Zener breakdown.
Depletion Region	The depletion region is thicker during avalanche breakdown.	The depletion region is thinner during avalanche breakdown.
Junction	The junction is destroyed.	The junction is larger and not destroyed.
Electric Field	The electric field across the diode is weak	The electric field across the diode is stronger and in the opposite direction
Produces	Pairs of electron and hole.	Electrons.
Doping	Avalanche breakdown is predominant in diodes that are lightly doped.	Zener breakdown occurs in heavily doped diodes and much before the avalanche diodes.
Reverse potential	High	Low
Breakdown Voltage	Directly proportional to temperature.	Inversely proportional to temperature.
After Breakdown	Voltage varies.	Voltage remains constant

### 2.3.3 Diode Equivalent Circuit

Equivalent circuits are circuits with passive circuit elements and active circuit elements that replicate the behavior of the device. The basic model of the equivalent circuit is given in Figure 2.5.

#### Ideal diode



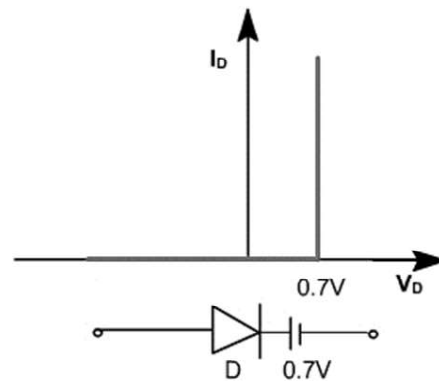
**Fig. 2.5** (a) Basic Equivalent Circuit Model of the Diode,  
(b) Ideal Diode Characteristics

The application of diode is it can be used as a switch on both On and OFF condition. The ON condition of the diode is replaced as a switch in the closed

condition and the OFF condition of the diode is replaced as a switch in OFF condition. Hence, from the characteristics, when the diode is ON, the current conduct indefinitely with a zero applied voltage, i.e., it acts as a short circuit. When the diode is OFF, the diode acts as an open circuit and hence the current across the diode is zero with any voltage applied to it.

### An ideal diode with a cut in voltage and zero internal resistance

But practically, ideal diodes does not exist and hence, on the introduction of the cut in voltage property of the diode, the equivalent circuit gets modified as shown in Figure 2.6.



**Fig. 2.6** A Simplified Model of the Diode

The approximate equivalent circuit model with only the cut in voltage is also called as a simplified model. In the forward bias, practical diodes offer, cut in barrier potential or knee voltage potential of 0.7 V for silicon diodes and 0.3 V for Germanium diodes. Hence, the equivalent circuit is modified to accommodate the ideal diode with a battery presumed to be offering a barrier voltage of 0.7 V. Also, it's to be noted that, the battery is connected in reverse polarity of the applied voltage during the forward biasing of the diode. The barrier potential voltage must oppose the applied battery potential.

During reverse bias, the model follows the ideal diode model of approximation and hence it is represented as an open circuit. The model under discussion offers no internal resistance both during forward bias and reverse bias. Hence, the characteristics does not offer any slope representation.

### Piecewise linear model of a diode

The piecewise linear model of the diode offers internal forward resistance,  $R$ . The change in characteristics is as shown in Figure 2.7 with knee voltage represented as  $v_0$ .

## NOTES

## NOTES

## Piecewise linear diode model



## Characteristics

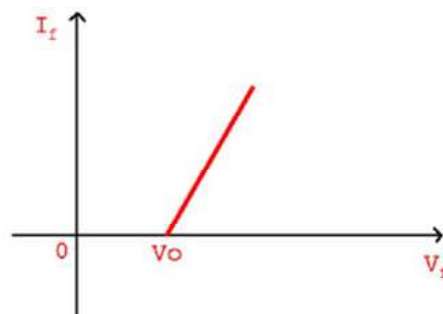


Fig. 2.7 Piecewise Linear Model of the Diode

The addition of internal forward resistance of the diode offers slope after the threshold or knee voltage of the diode.

## 2.3.4 Application of Diode

Diodes are used in applications such as DC power supplies. DC power supplies provide constant DC voltage output. It takes AC input voltage and with the help of a transformer, rectifiers, filters, and regulators, it converts the input AC to DC. The rectifier inside the DC power supply is the important circuitry behind the AC to DC conversion. A simplified block diagram that represents the DC power supply is given in Figure 2.8.

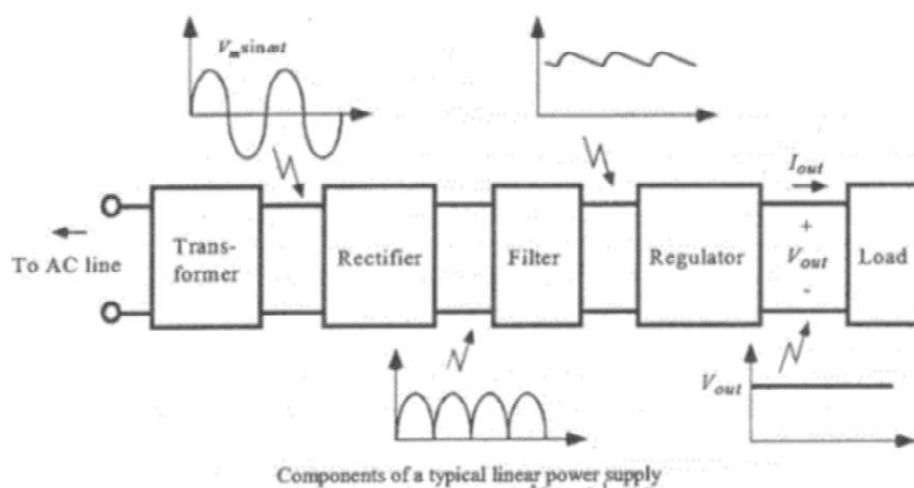


Fig. 2.8 DC Power Supply

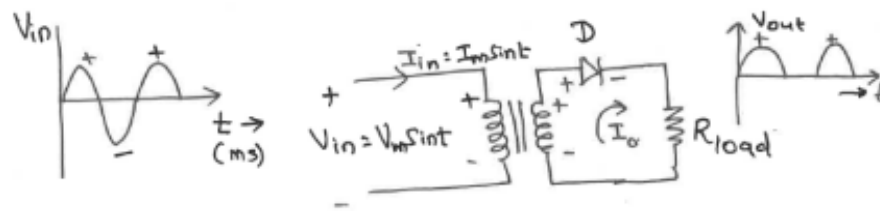
The rectifiers that convert AC voltages to DC voltages consists of diodes. Based on the output waveform and based on the components used rectifiers are classified as below.

- (a) Half-wave rectifiers
- (b) Full wave rectifiers
- (c) Centre tapped full wave rectifiers
- (d) Bridge rectifiers

## NOTES

### Half-Wave Rectifiers

Half-wave rectifiers as the name implies rectifies AC to DC voltage in only for half the wave cycle. Half-wave rectifiers contain a step-down transformer, a diode, and a load resistance. The circuit diagram for half wave rectifier is as shown in Figure 2.9 below



**Fig. 2.9** Half Wave Rectifier

### Working

The input voltage is an Alternating Current (AC) voltage given as

$$V_{in} = V_m \sin t$$

Since the input voltage is an AC voltage, the input current is also an AC current given as

$$I_{in} = I_m \sin t$$

During the positive input cycle, the transformer steps down the input voltage. The secondary side of the transformer experiences the potential as shown in Figure 2.9. The anode side of the diode experiences a positive voltage and cathode side of the diode experiences a negative voltage. This makes the diode forward biased and the diode conducts. The current flows through the diode and through the load resistor. This current is the output current represented as  $I_o$ . Output voltage is experienced across the load resistor when current flows through it and hence an output voltage similar to the input voltage cycle is obtained.

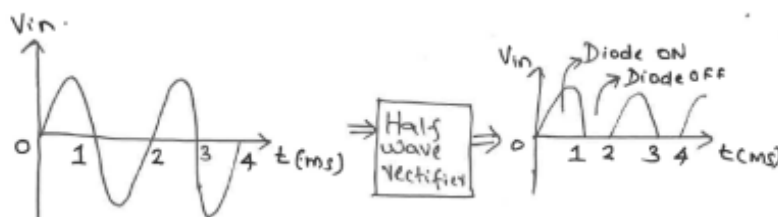
During the negative cycle of the input voltage, the primary side and the secondary side of the transformer, experiences  $-/+$  polarity across them. That is, the anode experiences negative voltage and cathode experience positive voltage. This polarity makes the diode reverse biased leading the non-conduction of the diode. This is similar to the open circuit condition. As no current flows through the



diode, there is no current through the load resistor as well. Therefore the output voltage across the load resistor is zero.

The input-output voltage waveform for a half wave rectifier is as shown in Fig 2.10.

## NOTES



**Fig 2.10** Input Output Wave Form for a Half Wave Rectifier

Let the input voltage be

$$v_{in} = v_{\max} \sin \omega t$$

$$I_{in} = I_{\max} \sin \omega t$$

where

$$I_{\max} = \frac{V_{\max}}{R_L}$$

In the positive cycle, that is  $0 \leq \omega t \leq \pi$ ,

$$I_l = I_{\max} \sin \omega t$$

In the negative cycle, that is  $\pi \leq \omega t \leq 2\pi$ ,

$$I_l = 0$$

Average Value:

$I_{av}$ :

$$\begin{aligned} I_{av} &= \frac{1}{2\pi} \int_0^{2\pi} I_l d(\omega t) \\ &= \frac{1}{2\pi} \left[ \int_0^{\pi} I_l d(\omega t) + \int_{\pi}^{2\pi} I_l d(\omega t) \right] \\ &= \frac{1}{2\pi} \left[ \int_0^{\pi} I_l d(\omega t) + 0 \right] \\ &= \frac{1}{2\pi} \left[ \int_0^{\pi} I_{\max} \sin \omega t d(\omega t) \right] \\ I_{av} &= \frac{I_{\max}}{\pi} \end{aligned}$$

$V_{av}$ :

$$V_{av} = I_{av} \times R_{load}$$

$$= \frac{I_{max}}{\pi} \times R_{load}$$

RMS Value:

 $I_{rms}$ :

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_t^2 d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{\pi} I_t^2 d(\omega t) + \int_{\pi}^{2\pi} I_t^2 d(\omega t) \right]}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{\pi} I_t^2 d(\omega t) + 0 \right]}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{\pi} I_{max}^2 \sin^2 \omega t d(\omega t) \right]}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{\pi} I_{max}^2 \left( \frac{1}{2} (1 - \cos 2\omega t) \right) d(\omega t) \right]}$$

$$= \sqrt{\frac{I_{max}^2}{2\pi} \left[ \int_0^{\pi} \frac{1}{2} d(\omega t) - \int_0^{\pi} \frac{1}{2} \cos 2\omega t d(\omega t) \right]}$$

$$= \sqrt{\frac{I_{max}^2}{2\pi} \left[ \frac{\pi}{2} - 0 \right]}$$

$$I_{rms} = \frac{I_{max}}{2}$$

 $V_{rms}$ :

$$V_{rms} = I_{rms} \times R_{load}$$

$$= \frac{I_{max} R_{load}}{2}$$

**Peak Inverse voltage**

Peak Inverse voltage (PIV) is defined as the maximum negative voltage appearing across the reverse biased diode.

$$PIV_{HW} = V_{max}$$

**Ripple factor**

The ripple factor is defined as the ratio of the output AC components to output DC components of voltage/current.

**NOTES**

The total output current from a half wave rectifier contains both AC and DC components. Therefore,

$$I_{rms}^2 = I_{ac}^2 + I_{dc}^2$$

$$I_{ac}^2 = I_{rms}^2 - I_{dc}^2$$

$$= I_{dc}^2 \left\{ \frac{I_{rms}^2}{I_{dc}^2} - 1 \right\}$$

It is denoted as  $\Gamma$

$$\Gamma_{HW} = \frac{V_{ac}}{V_{dc}} \text{ or } \frac{I_{ac}}{I_{dc}}$$

$$\Gamma_{HW} = \frac{I_{ac}}{I_{dc}} = \sqrt{\left( \frac{I_{rms}^2}{I_{dc}^2} - 1 \right)}$$

$$= \sqrt{\left( \frac{\frac{I_{max}}{2}}{\frac{I_{max}}{\pi}} - 1 \right)}$$

$$= 1.21$$

### Efficiency

The efficiency of the half-wave rectifier is defined as the ratio of the output DC power to the input AC power. It is given as

$$\eta = \frac{P_{dc} (output)}{P_{ac} (input)}$$

Where

$$P_{dc} = I_{dc}^2 R_{load}$$

$$= \frac{I_{max}^2}{\pi^2} R_{load}$$

$$P_{ac} = P_{input} = I_{ac}^2 (R_{load} + R_{diode})$$

$$= \frac{I_{max}^2}{2^2} (R_{load} + R_{diode})$$

$$\eta = 4/\pi^2 \left( \frac{R_{load}}{R_{load} + R_{diode}} \right)$$

$$\approx 0.406$$

$$\% \eta = 40.6\%$$

### NOTES

## Summary

Semiconductor Diode

Average current	$I_{av} = \frac{I_{max}}{\pi}$
RMS current	$I_{rms} = \frac{I_{max}}{2}$
Peak Inverse Voltage (PIV)	$PIV_{HW} = V_{max}$
Ripple Factor	$\Gamma_{HW} = 1.21$
Efficiency (%)	$\% \eta = 40.6\%$

## NOTES

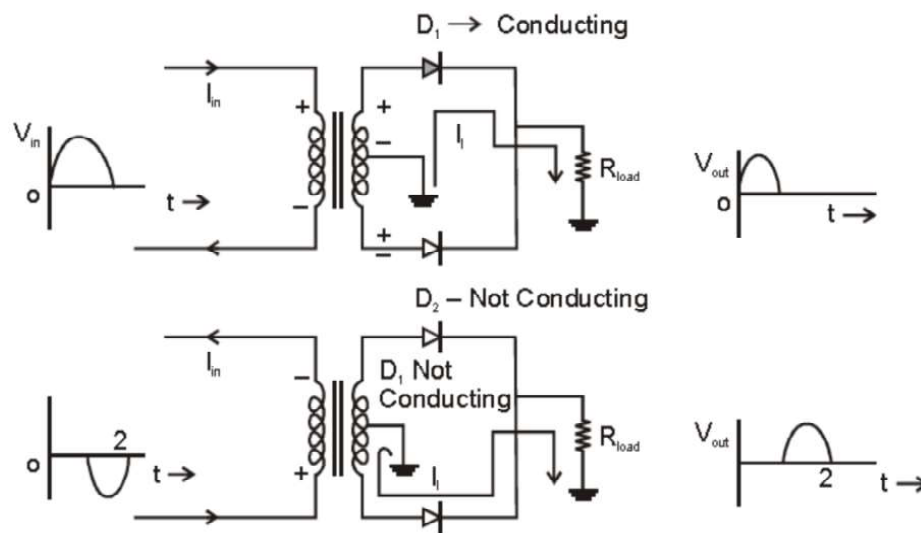
### Full Wave Rectifiers

In full wave rectifiers, the input AC voltage is rectified in both the cycles. Full wave rectifiers are of two types

1. Center tapped full wave rectifiers
2. Bridge rectifiers

### Center Tapped Full Wave Rectifiers

These types of rectifiers employ a center tapped transformer, two diodes, and a load resistor. The circuit diagram of such type of rectifiers is shown in Figure 2.11.



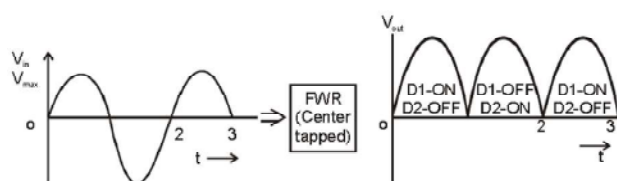
**Fig. 2.11** (a) Positive Cycle of Full Wave Rectifier in Center Tapped Transformer  
(b) Negative Cycle of Full Wave Rectifier in Center Tapped Transformer

### Working

Let the two diodes be diode  $D_1$  and diode  $D_2$ . During the positive cycle, the center tapped transformer induces a polarity as shown in Figure 2.11a. This induced polarity makes the diode  $D_1$  forward biased and  $D_2$  reverse biased. Diode  $D_2$ ,

## NOTES

while reverse biased acts an open circuit and diode due to forward biased acts as a short circuit. Hence the direction of flow of current will be as shown in Figure 2.11a. Observing the direction of current flow across the output load resistor, the current flows from the circuit to the ground through the resistor. Since the input voltage is sinusoidal, the primary voltage, secondary voltage and secondary output current are also sinusoidal in nature. During the negative input cycle, the induced polarity on the secondary of the center tapped transformer will reverse which makes the diode  $D_1$  reverse biased and  $D_2$ —forward biased. Now, the direction of flow of current will be from ground to load resistor through diode  $D_2$ . In both the cases, the direction of the current through the load resistor is same and hence the output voltage cycle across the resistor is in the same direction and hence the input-output cycle of the waveforms as shown in Figure 2.12 is obtained.



**Fig. 2.12** The Input-Output Waveform of a Centre Tapped Transformer

$I_{av}$ :

$$I_{av} = \frac{I_{max}}{\pi} \times 2$$

$$I_{av} = \frac{2I_{max}}{\pi}$$

$I_{rms}$ :

$$I_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} I_l^2 d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{\pi} I_l^2 d(\omega t) + \int_{\pi}^{2\pi} I_l^2 d(\omega t) \right]}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{2\pi} I_{max}^2 \sin^2 \omega t d(\omega t) \right]}$$

$$= \sqrt{\frac{1}{2\pi} \left[ \int_0^{2\pi} I_{max}^2 \left( \frac{1}{2} (1 - \cos 2\omega t) \right) d(\omega t) \right]}$$

$$= \sqrt{\frac{I_{max}^2}{4\pi} \left[ \int_0^{2\pi} d(\omega t) - \int_0^{2\pi} \cos 2\omega t d(\omega t) \right]}$$

$$= \sqrt{\frac{I_{max}^2}{2}}$$

$$I_{rms} = \frac{I_{max}}{\sqrt{2}}$$

### Peak Inverse voltage

In full wave rectifier, when one diode  $D1$  is conducting,  $D2$  is reverse biased and when  $D2$  is conducting,  $D1$  is reverse biased.

$$PIV_{FW} = 2V_{max}$$

### Ripple factor

$$\begin{aligned}\Gamma_{FW} &= \frac{I_{ac}}{I_{dc}} = \sqrt{\left(\frac{I_{rms}^2}{I_{dc}^2} - 1\right)} \\ &= \sqrt{\left(\frac{\frac{2I_{max}}{\pi}}{\frac{I_{max}}{\sqrt{2}}} - 1\right)} \\ &= 0.48\end{aligned}$$

Lower the ripple factor, lesser is the output waveform oscillations during the rectification process. Lesser value of ripple factor ideally equal to zero is preferred.

### Efficiency

$$\eta = \frac{P_{dc}(output)}{P_{ac}(input)}$$

Where

$$P_{dc} = I_{dc}^2 R_{load}$$

$$= \frac{4I_{max}^2}{\pi^2} R_{load}$$

$$P_{ac} = P_{input} = I_{ac}^2 (R_{load} + R_{diode})$$

$$= \frac{I_{max}^2}{2} (R_{load} + R_{diode})$$

$$\eta = 8/\pi^2 \left( \frac{R_{load}}{R_{load} + R_{diode}} \right)$$

$$\approx 0.812$$

$$\% \eta = 81.2\%$$

### NOTES

Summary

NOTES

Average current	$I_{av} = \frac{2I_{max}}{\pi}$
RMS current	$I_{rms} = \frac{I_{max}}{\sqrt{2}}$
Peak Inverse Voltage (PIV)	$PIV_{FW} = 2V_{max}$
Ripple Factor	$\Gamma_{FW} = 0.48$
Efficiency (%)	$\% \eta = 81.2\%$

Bridge rectifiers

Bridge rectifiers are also full wave rectifiers. The circuit diagram of the bridge rectifier is shown in Figure 2.13. Bridge rectifier employs a transformer, 4 diodes, and load resistor.

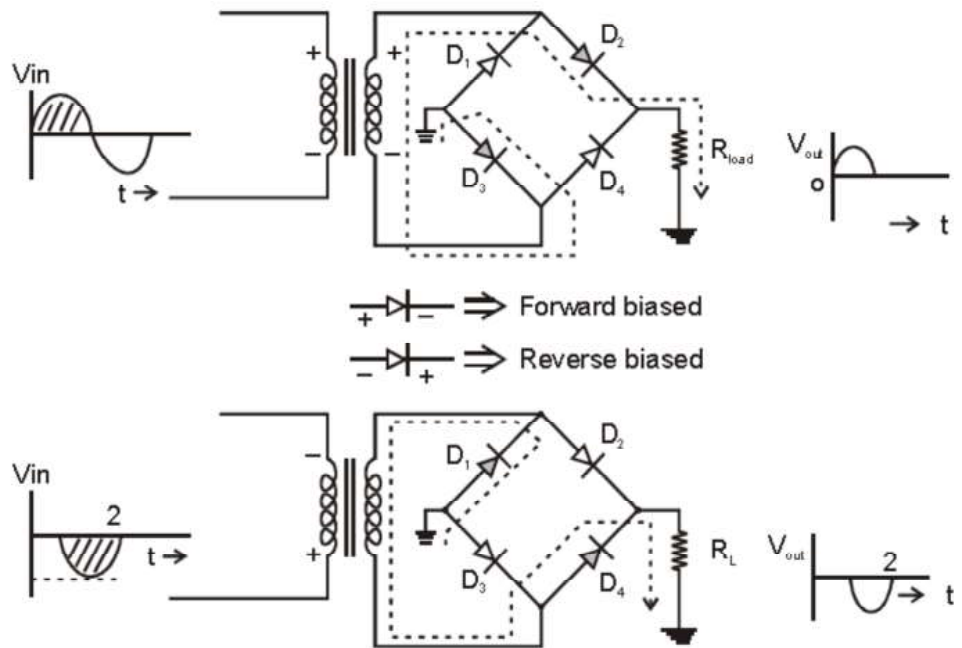
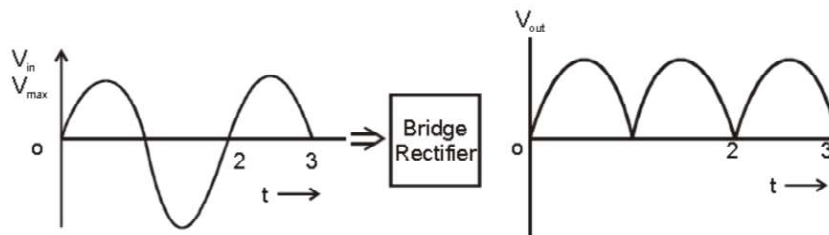


Fig. 2.13 Bridge Rectifier

During the positive cycle, the primary and secondary transformer windings are induced with the polarity as shown in Figure 2.13. The diodes  $D_2$  and  $D_3$  are forward biased as the anodes of both the diodes experience a positive polarity from the secondary terminal of the transformer. At the same time,  $D_1$  and  $D_4$  are reverse biased as the cathodes of both the diodes experience positive polarity. Therefore, the circuit path consisting of diodes  $D_2$  and  $D_3$  are equivalently short

circuited, whereas  $D1$  and  $D4$  are open circuited. The current flows through the diode  $D3$ , transformer, diode  $D2$  and the load resistor during positive cycle. The direction of the current flow is shown in dotted lines in the Figure 2.13. During negative cycle, the diodes  $D2$  and  $D3$  are reverse biased, whereas  $D1$  and  $D4$  are forward biased. Therefore, the circuit path consisting of diodes  $D2$  and  $D3$  are equivalently open circuited, whereas  $D1$  and  $D4$  are short circuited. The current in the circuit now flows through  $D4$ , transformer, diode  $D1$  and the load resistor during the negative cycle. In both the cycles, the direction of current through the load resistor is the same and hence the rectified output waveform as shown in Figure 2.14 is obtained.



**Fig. 2.14** The Input-Output Waveform of a Bridge Type Transformer

The average value, RMS value, ripple factor, and efficiency expressions are the same as derived for the center tapped transformer and given as below:

$$I_{av} = \frac{2I_{max}}{\pi}$$

$$I_{rms} = \frac{I_{max}}{\sqrt{2}}$$

$$PIV_{FW} = V_{max}$$

$$\Gamma_{FW} = 0.48$$

$$\eta \approx 0.812$$

It should be observed that the PIV voltage of the bridge rectifier is  $V_{max}$  as against the centre tapped transformer rectifier value of  $2V_{max}$ .

Bridge rectifiers are advantageous than the other types of rectifiers for the following reasons:


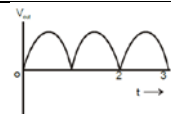
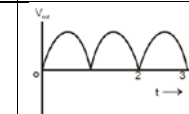
1. They provide rectification in both the cycles
2. They have higher rectification efficiency
3. They have lower ripple factor
4. They have lower PIV voltage
5. They do not require bulk transformers to operate

## NOTES



## Comparison of Rectifiers

## NOTES

Sl. No	Metrics parameter	Half wave rectifier	Centre tapped transformer rectifier	Bridge rectifier
1	$I_{av}$	$\frac{I_{max}}{\pi}$	$\frac{2I_{max}}{\pi}$	$\frac{2I_{max}}{\pi}$
2	$I_{rms}$	$\frac{I_{max}}{2}$	$\frac{I_{max}}{\sqrt{2}}$	$\frac{I_{max}}{\sqrt{2}}$
3	PIV	$V_{max}$	$2V_{max}$	$V_{max}$
4	Ripple factor	1.21	0.48	0.48
5	Rectification Efficiency	40.6%	81.2%	81.2%
6	Is the transformer required?	May be required	Yes	May be required
7	Type of transformer	Step down	Center tapped	Step down
8	Number of diodes	1	2	4
9	Output waveform			

## Filters

The rectified output voltage from the rectifier is not a pure DC output voltage, hence shaping of the waveform is required. Shaping includes converting the oscillating cycle in the positive direction to a pure DC waveform. This step is accomplished using a filter circuit and a regulator circuit. The shaped waveform after a filter circuit is shown in Figure 2.15.

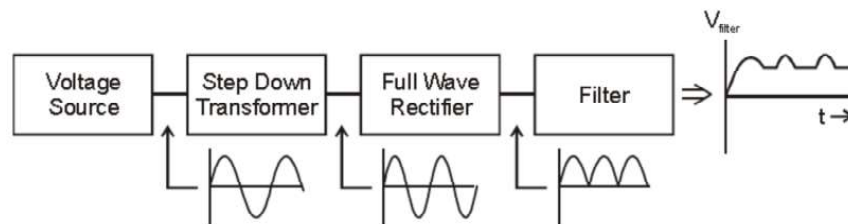


Fig. 2.15 Block Diagram of a Filter Circuit

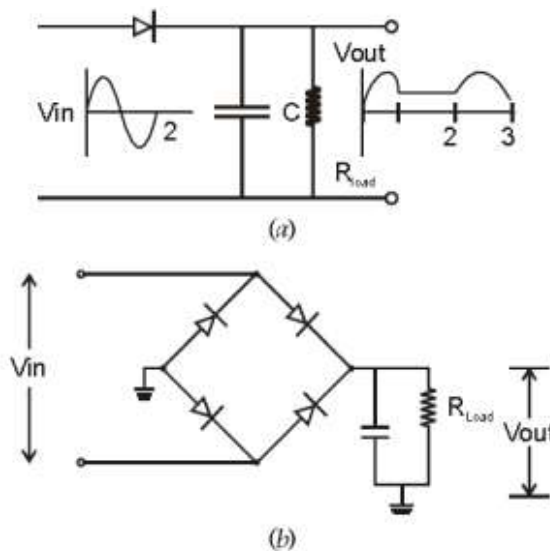
Filter circuit or network may consist of a capacitor, a combination of capacitor and inductor, a  $\pi$  network etc. Also, the ripple factor of the half wave rectifier and full wave rectifier are 1.21 and 0.48 respectively. The lesser the ripples or in other words, lesser the value of the ripple factor, better is the rectified output voltage. Based on the structure and components used in filter circuits they may be classified as

- Capacitor filter
- Inductor filter

- network filter
- network filter
- L section filter

### Capacitor filter

The circuit diagram employing half wave rectifier and a capacitor filter is shown in Figure 2.16a. Similarly, a circuit diagram employing a bridge rectifier and a capacitor filter is shown in Figure 2.16b.



**Fig. 2.16** (a) Half Wave Rectifier with C Filter, (b) Full Wave Rectifier with RC Filter

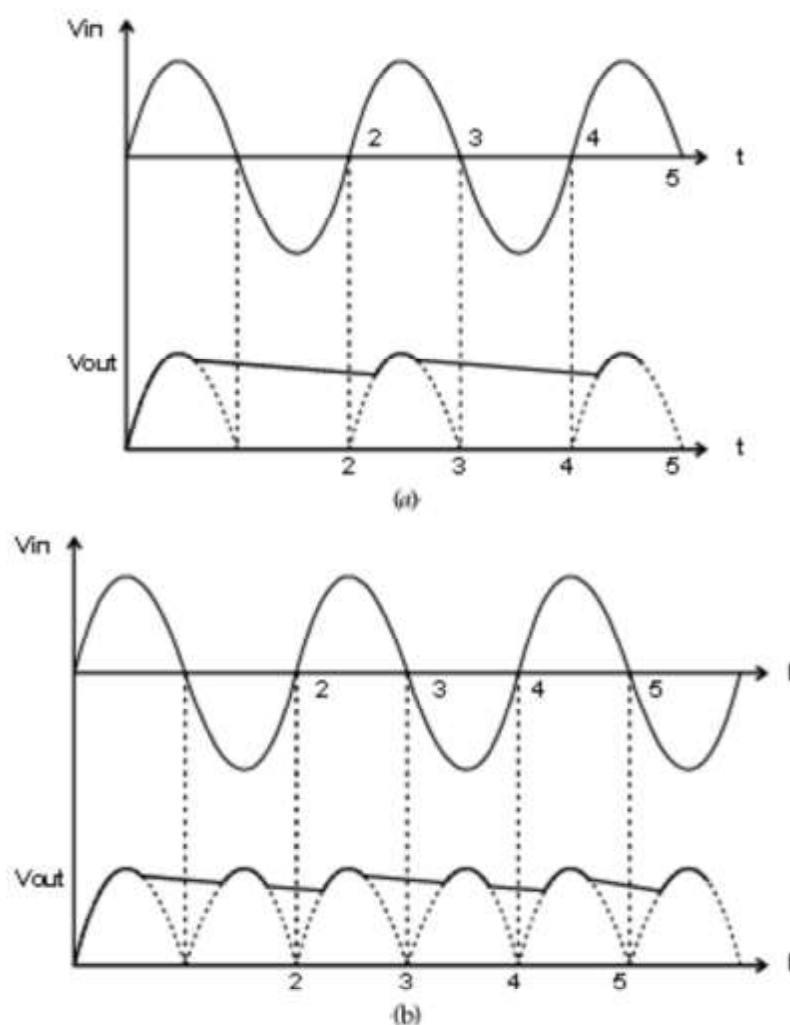
### Working (HWR with Capacitor filter)

During the forward positive cycle, when the diode is forward biased, the current flows through the diode and load resistor. During this cycle, the capacitor gets charged forcing the output voltage to follow the capacitor voltage, since capacitor and load resistor are connected in parallel. The charging time depends on the  $\tau = R_d C$  of diode resistance and capacitor.

During the negative cycle, when the diode is reverse biased, the diode acts as an open circuit and the charge stored in the capacitor discharges through the load resistor. The discharge depends on the  $R_L C$  constant of the load resistor and the capacitor. From the output waveform of Figure 2.17, the rectifier output voltage is shaped to a near DC voltage thereby achieving a better smaller ripple factor. Figure 2.17 represents the input-output waveforms for both half and full wave rectifier filter circuits. In half wave rectifier filter circuit, the discharging time is longer for one complete negative cycle of the rectifier input, whereas in full wave rectifier filter circuit, the discharging time constant is from one peak to the next immediate peak of the rectifier output. Full wave rectifier filter output is closer to a DC waveform than the half wave counterpart.

### NOTES

## NOTES



**Fig. 2.17** Input-Output Waveform for a) HWR with C Filter, b) FWR with C Filter.

The ripple factor for an FWR with capacitor filter is given as

$$\Gamma = \frac{1}{4\sqrt{3}fCR_{load}}$$

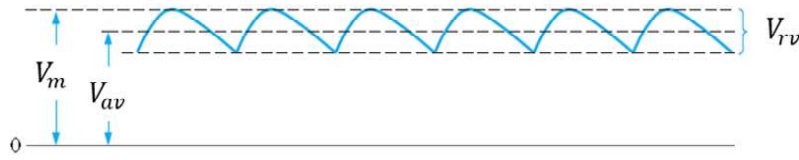
Where  $f$  = input voltage frequency, (normally 50 Hz)

$C$  = Capacitor value of the filter ( $\mu F$ )

$R_{load}$  = load resistor in ohms

### Proof

Let  $V_m$  be the maximum amplitude of the rectified voltage and  $V_{rv}$  be the ripple voltage peak to peak magnitude. Therefore the actual amplitude will be equivalent to the difference between the maximum amplitude and the ripple voltage of the filtered waveform. Hence, from the Figure 2.18,  $V_{dc}$  voltage is given as



**Fig. 2.18** Ripple Voltage Waveform from the Filtered Circuit

$$V_{av} = V_m - \frac{V_{rv}}{2}$$

$V_{rms}$  voltage has both dc and ac components and hence,

$$V'_{rms} = \frac{V_{rv}}{2\sqrt{3}}$$

The relation for capacitance  $C$  is given as

$$C = Q/V$$

Therefore,

$$V = \frac{Q}{C} = \frac{I_{av} \left( \frac{T}{2} \right)}{C} = \frac{I_{av}}{2fC}$$

$$V_{av} = V_m - \frac{I_{av}}{4fC}$$

Ripple factor,

$$\Gamma = \frac{V'_{rms}}{V_{av}}$$

$$\Gamma = \frac{I_{av}}{2\sqrt{3} \times 2fCV_{av}}$$

$$\Gamma = \frac{I_{av}}{2\sqrt{3} \times 2fC(I_{av}R_{load})}$$

$$\Gamma = \frac{1}{4\sqrt{3} \times fCR_{load}}$$

### LC Filter

The circuit diagram of an LC filter is as shown in Figure 2.19. The LC filter consists of  $L$  in series with parallel RC combination. The capacitor in the LC works as described in RC filter, that is it charges during the positive cycle and discharges in the negative cycle. The rate of charging is now affected by the series inductance. Since current across inductance does not change instantly, the charging of the capacitor also does not occur instantly, but charges at a differential rate with respect to time ( $dv/dt$ ). The ripple factor for a LC filter is given as

### NOTES

## NOTES

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$I_{ac} = \frac{4V_{max}}{3\sqrt{2}\pi(\omega L)}$$

$$V_{ac} = I_{ac} \times \left( \frac{1}{\omega C} \right)$$

$$= \frac{4V_{max}}{3\sqrt{2}\pi(\omega^2 LC)}$$

$$\Gamma = \frac{\left( \frac{4V_{max}}{3\sqrt{2}\pi(\omega^2 LC)} \right)}{\frac{2V_{max}}{\pi}} = \frac{\sqrt{2}}{3} \frac{1}{\omega^2 LC}$$

$$\Gamma = \frac{0.4714}{\omega^2 LC}$$

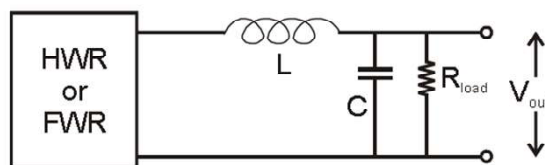
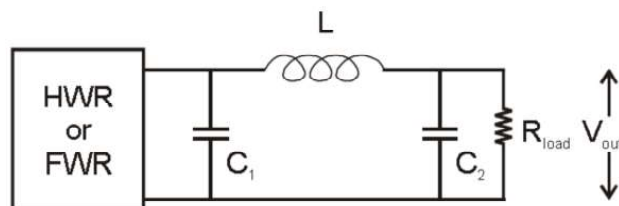


Fig. 2.19 LC Filter

 **$\pi$  Filter**

The block diagram of a  $\pi$  network is shown in Figure 2.20. The  $\pi$  network consists of two shunt branch and a series branch. The shunt branches consists of capacitors  $C_1$  and  $C_2$ , the series branch consists of inductor  $L$ . The combination of  $C_1$ ,  $C_2$  and  $L$  performs the filtering operation. Following similar steps for other filters discussed earlier, the ripple factor is given as

$$\Gamma = \frac{\sqrt{2}}{8} \frac{1}{\omega^3 LC_1 C_2 R_{load}}$$

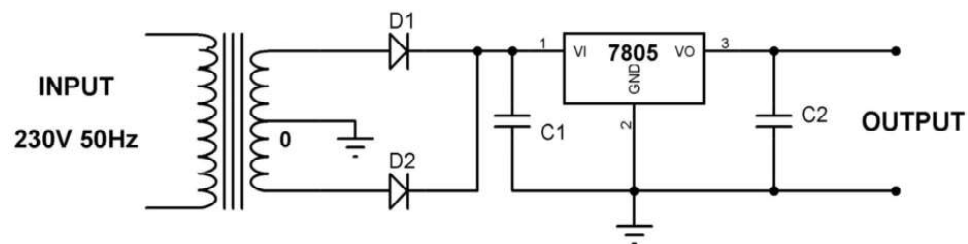
Fig. 2.20  $\pi$  Filter

## Regulators

The output voltage obtained from the filter circuit is still not in a pure DC form, hence as a last stage of the rectification process, regulators are used to obtaining a pure DC output voltage waveform. Regulators are generally integrated circuits (ICs). Some of the IC regulators are as below with a regulated output voltage. Most ICs are three terminal devices, consisting of input terminals, output terminals, and a ground terminal. These ICs are well protected against thermal protection, short circuit protection etc. These ICs have a reference voltage signals to operate. They are available at different levels of voltages that include positive and negative voltages as depicted in the table below. For additional surge protection for this voltage regulator ICs, and also to obtain pure dc output voltage waveform, capacitors are connected at the last stage in parallel with the load resistor  $R_{load}$  after the ICs as shown in Figure 2.21. The regulator circuit shown in Figure 2.21 employs center tapped full wave rectifier. The capacitors C1 offers filtering to the rectified output and capacitor C2 offers surge protection for the regulator IC.

## NOTES

IC	Output voltage	IC	Output voltage
7802	+ 2V	7902	- 2V
7805	+ 5V	7905	- 5V
7810	+ 10V	7910	- 10V
7812	+ 12V	7912	- 12V



**Fig. 2.21** IC Regulator with Surge Protection using Center Tapped Transformer Rectifier

### Check Your Progress

- What is static resistance?
- What is the mathematical expression for the diode current as a dependent function on diode voltage that depicts the v-i characteristics of the diode?
- What is avalanche breakdown?
- What is Zener breakdown?
- What is peak inverse voltage?
- What is a rectifier?

## 2.4 ZENER DIODE

### NOTES

Zener diodes are special purpose diodes that are used to operate in the reverse biased condition. The Zener diodes are similar to  $p-n$  junction diodes with a difference in the doping process. The Zener diodes are heavily doped such that the impurity concentration alters the breakdown voltage of the diode. Heavy doping results in a reduction of the reverse breakdown voltage of the diodes. The difference between the normal  $p-n$  junction diodes and Zener diodes is the reverse breakdown voltage of Zener is much smaller when compared to the  $p-n$  junction diodes. Zener diodes are operated in the reverse breakdown region. Zener diodes can withstand a large change in reverse currents for a minimal change in reverse voltages, hence Zener diodes are preferred as voltage regulators. In other words, the Zener diode when connected in reverse bias, they can hold the voltage across the terminal for a large change in reverse current across it.

The circuit symbol of the Zener diode is shown in Figure 2.22. The circuit symbol is similar to the  $p-n$  junction diode except for the cathode portion of the symbol is modified to represent “Z” of Zener.

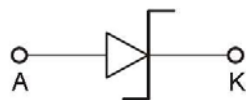
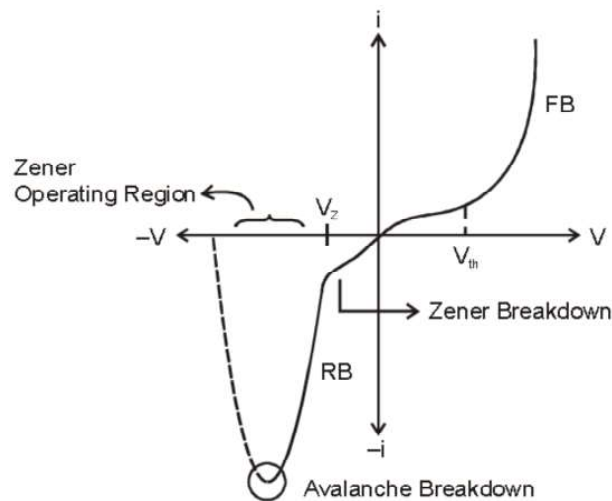


Fig. 2.22 Zener Diode Symbol

The  $v-i$  characteristics of the Zener diodes exhibit similar characteristics that of the normal  $p-n$  junction diode, but the difference in the reverse break down voltage. The  $v-i$  characteristics of the Zener diode are as shown in Figure 2.23. In the forward bias region for positive input voltage, after the threshold voltage or knee voltage, the Zener diode, similar to the  $p-n$  junction diode increase abruptly and behave as a short-circuited element. In the reverse biased region, for a negative input voltage across the Zener diode, they exhibit two types of breakdown voltages. They are

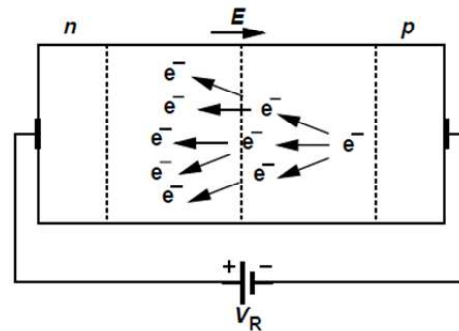
1. Avalanche breakdown voltage
2. Reverse breakdown voltage

Reverse breakdown voltage occurs due to the flow of the minority carriers as a result of the breakdown of the  $p-n$  junction. The minority carrier current increases abruptly even for a slight change in the reverse applied voltage. For a large reverse bias voltage beyond the breakdown, Zener has the capacity to hold the voltage even for a large change in reverse minority current. The reverse voltage  $V_z$  at which the reverse breakdown occurs is called as Zener voltage.



**Fig. 2.23** *V-I Characteristics of the Zener Diode*

Avalanche breakdown voltage occurs when the reverse input voltage is further increased beyond the reverse breakdown voltages. The conducting minority carriers achieve huge momentum bombarding other atoms resulting in an avalanche of electron multiplication through bombarding. Beyond avalanche breakdown, the diode results in damage. The avalanche breakdown inside the diodes is represented in Figure 2.24. The process of multiplication of electrons due to the bombardment of excited electrons is called avalanche multiplication. The resulting breakdown due to continuous electron multiplication is called avalanche breakdown.



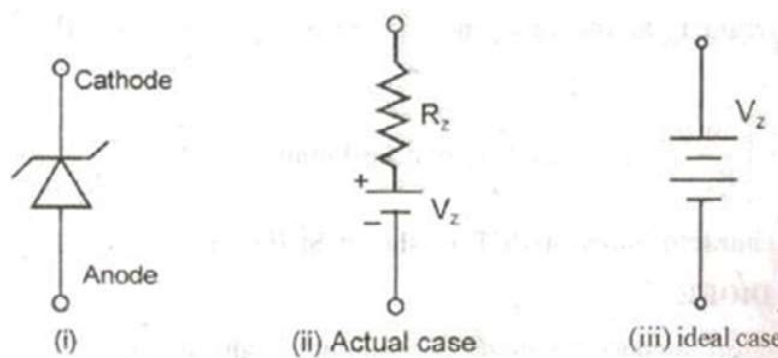
**Fig. 2.24** *Avalanche inside a Diode*

The equivalent circuit of the Zener diode is given in Figure 2.25. Under ideal condition, the Zener diode is equivalent to a voltage source generating a Zener voltage  $V_z$ . Considering the internal resistance of the Zener diode, the practical equivalent circuit is given in Figure 2.25.

## NOTES



## NOTES



**Fig. 2.25** Equivalent circuit of a Zener Diode

The power dissipated across the Zener diode is given as

$$P_{Z(max)} = V_Z \times I_{Z(max)}$$

Where,  $I_z$  is the reverse current that flows through the Zener diode.

### Application of Zener diode

Zener diode finds many applications such as

- voltage regulators
- wave shaping circuits
- Clippers and clampers.

#### 2.4.1 Zener Diode as a Voltage Regulator

##### Types of voltage regulators

There are different types of voltage regulators based on the type of configuration of the voltage regulator elements used. The voltage regulator elements may be a Zener diode, transistor, and its various configurations, operational amplifiers etc.

Following are the types of the voltage regulators based on whether the regulator elements are connected in series, shunt or in a combination of both. They are

- shunt regulators
- series regulators
- SMPS

Shunt and series regulators are further classified as given below.

##### Shunt regulators

- Zener regulator
- Transistorized shunt regulator

## Series regulators

- Emitter follower regulator
- The controlled transistor series voltage regulator
- Transistor current regulator
- Variable feedback regulator

Switched mode regulators or switched mode power supply (SMPS)

## NOTES

### Shunt Voltage Regulator

A voltage regulator employing a Zener diode is shown in Figure 2.26. Since the Zener diode is connected in parallel with the load resistor, such type of voltage regulators are called as shunt voltage regulators. The objective of the voltage regulator is to provide to constant output voltage across the load resistor despite the change in input voltage or output resistance. The Zener diode is reverse biased by the input voltage. When the input voltage is increased, the current from the source voltage also increases. The output current across the fixed load resistor remains constant, whereas, in order to obey Kirchhoff's current law (KCL), the increased current, flows through the Zener diode. Though there is an increase in the current through Zener diode, since they operate in the reverse breakdown region, the output voltage which is the Zener voltage does not vary. Hence the circuit shown in Figure 2.26 is used as a voltage regulator.

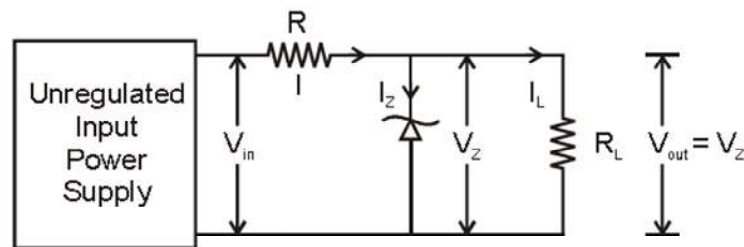


Fig. 2.26 Zener Diode in a Series Voltage Regulator

### Working of a voltage regulator

Let current  $I$  flows through the series resistance. The series resistance is also called as a current limiting resistance. The load current  $I_L$  flows through the load  $R_L$  at a constant Zener voltage  $V_Z$ . Current through the Zener diode is  $I_Z$ .

Total current in the circuit is

$$I = I_Z + I_L$$

Input voltage from the source is determined by applying KVL in loop 1,

$$V_{in} = V_Z + IR$$

$$V_{in} = V_Z + (I_Z + I_L) R$$

## NOTES

When there is an increase in the load current  $I_L$ , the Zener current  $I_Z$  decreases to maintain constant input current  $I$ . The change in  $I_Z$  does not make a significant change in  $V_Z$ , since they operate in the reverse breakdown region. Hence from the  $V_{in}$  equation, both  $V_Z$  and  $IR$  remains constant, thereby maintaining the output voltage  $V_{out} = V_Z$ .

**Regulation**

There are two types of regulations of voltage. They are line regulation and voltage regulation.

**Line regulation:** In line regulation, the output load resistance is varied with the fixed input voltage. Since the load resistor is fixed, the output voltage is constant till the value of the load resistance is above a minimum value.

$$\%R = \frac{V_{No-load} - V_{Full-load}}{V_{No-load}} \times 100$$

**Voltage regulation:** In voltage regulation, as the name implies, the input voltage is changed and the change in the output voltage is observed with fixed input and output resistances.

$$\%R = \frac{dV_o}{dV_{in}} \times 100$$

**Fixed voltage DC power supply circuit**

Fixed DC power supply circuit consists of the following components:

- Transformer:
  - o The transformer may be a step-down or center tapped transformer
- Rectifier circuit
  - o Rectifier circuit may contain a half wave or a full wave rectifier circuit
- Filter circuit
  - o Filter circuit may employ a capacitor, inductor-capacitor,  $\pi$  type filters
- Regulator circuit
  - o These are voltage regulator IC's

**Sample Short Questions****1. Define and explain Peak Inverse Voltage (PIV)**

**Ans.** Peak inverse voltage is the maximum reverse voltage that can be applied to the **p-n** junction without damage to the junction. If the reverse voltage across the

junction exceeds its peak inverse voltage, the junction may be destroyed due to excessive heat.

## 2. Explain the terms knee voltage and breakdown voltage?

**Ans.** Knee voltage: The forward voltage at which the current through the *p-n* junction starts increasing rapidly is known as knee voltage. It is also called as cut-in voltage or threshold voltage. Breakdown voltage: It is the reverse voltage of a *p-n* junction diode at which the junction breaks down with sudden rise in the reverse current.

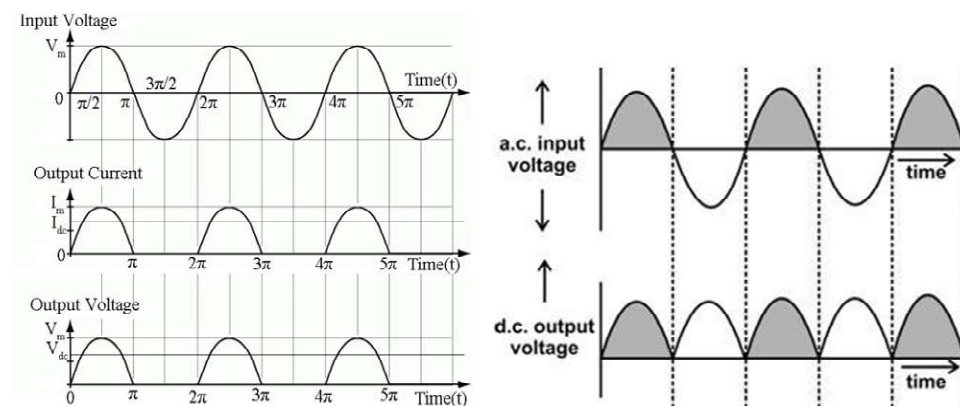
## 3. What is avalanche breakdown in *p-n* junction diode?

**Ans.** The avalanche breakdown takes place when both sides of the junction are lightly doped and due to this, the depletion layer is large. When the reverse bias voltage is increased the accelerated free electrons collide with the semiconductor atoms in the depletion region. Due to the collision, the covalent bonds are broken and electron-hole pairs are generated. These new charge carriers so produce acquire energy from applied potential and in turn produce additional carriers. This forms a cumulative process called avalanche multiplication, this causes the reverse current to increase rapidly. This leads to the breakdown of the junction known as avalanche breakdown.

## 4. Define Static resistance and Dynamic resistance?

**Ans.** The resistance offered by the diode to DC operating conditions is called “Static resistance” and the resistance offered by the diode to AC operating conditions is called “Dynamic resistance”.

## 5. Draw the input-output waveforms of half wave rectifier and full wave rectifier.



## NOTES

## NOTES

**6. Compare the half-wave rectifier, center tapped transformer rectifier and bridge rectifier for  $I_{av}$ ,  $I_{rms}$ ,  $PIV$ ,  $\eta$ , Ripple factor.**

Sl. No	Metrics parameter	Half wave rectifier	Centre tapped transformer rectifier	Bridge rectifier
1	$I_{av}$	$\frac{I_{max}}{\pi}$	$\frac{2I_{max}}{\pi}$	$\frac{2I_{max}}{\pi}$
2	$I_{rms}$	$\frac{I_{max}}{2}$	$\frac{I_{max}}{\sqrt{2}}$	$\frac{I_{max}}{\sqrt{2}}$
3	PIV	$V_{max}$	$2V_{max}$	$V_{max}$
4	Ripple factor	1.21	0.48	0.48
5	Rectification Efficiency	40.6%	81.2%	81.2%

**Check Your Progress**

10. What are Zener diode?
11. What are the types of breakdown in the Zener diode?

**2.5 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS**

1. The terminal connected to  $p$ -type is called anode that represents the positive polarity. and
2. The terminal connected to the  $n$ -type is called as cathode representing the negative polarity.
3. Biasing is the process of applying an external dc voltage to the device such that the device works under the proper operating region.
4. Static Resistance,  $R = \frac{V}{i} = \text{ohms}$
5. 
$$I = I_0 \left[ e^{\left( \frac{V}{\eta V_T} \right)} - 1 \right] A$$
6. The avalanche breakdown is a phenomenon of increasing the free electrons or electric current in semiconductor and insulating material by applying the higher voltage.
7. The process in which the electrons are moving across the barrier from the valence band of the  $p$ -type material to the conduction band of the lightly filled  $n$ -material is known as the Zener breakdown.

8. Peak Inverse voltage (PIV) is defined as the maximum negative voltage appearing across the reverse biased diode.
9. The rectifier is a circuit which converts AC to DC signal.
10. Zener diodes are special purpose diodes that are used to operate in the reverse biased condition. The Zener diodes are similar to  $p-n$  junction diodes with a difference in the doping process.
11. Zener diode exhibits two types of breakdown voltages. They are avalanche breakdown voltage and reverse breakdown voltage.

## NOTES

## 2.6 SUMMARY

- Rectifiers are classified as half wave and full wave rectifier.
- Half-wave rectifiers conduct for only one half of the cycle.
- Full wave rectifiers conduct for both the cycles of the input waveform.
- Full wave rectifiers may be center tapped or bridge rectifier.
- Center tapped transformers are bulky and costly as it employs transformers. Bridge rectifiers are preferred over center tapped rectifiers.
- The maximum negative voltage across a reverse biased diode is called a peak inverse voltage.
- The power supply consists of rectifiers, filters, and regulators.
- Filters are used to reduce the ripple voltage of the rectified output voltage from the rectifier.
- Regulators are IC's used to smoothen the DC output voltage from the filter.
- The Zener diode is made of heavily doped atoms.
- The Zener diode is mainly used as voltage regulators.
- Regulation may be classified as line regulation or load regulation.

## 2.7 KEY WORDS

- **Diode:** A semiconductor device with two terminals, typically allowing the flow of current in one direction only.
- **Voltage:** An electromotive force or potential difference expressed in volts.
- **Atom:** An atom is the smallest constituent unit of ordinary matter that has the properties of a chemical element. Every solid, liquid, gas, and plasma is composed of neutral or ionized atoms.
- **Rectifier:** An electrical device which converts an alternating current into a direct one by allowing a current to flow through it in one direction only.

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## 2.8 SELF ASSESSEMENT QUESTIONS AND EXERCISES

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### NOTES

#### Short-Answer Questions

1. List the applications of  $p$ - $n$  junction diode:
2. What is the need for the filter? Draw the typical output from a filter in a power supply circuit.
3. What are the types of rectifiers?
4. What are the different types of voltage regulators?
5. Draw the  $v$ - $i$  characteristics of a Zener diode.
6. Draw the block diagram of a DC power supply.

#### Long-Answer Questions

1. Draw the circuit diagram and explain the working of half wave rectifier and derive the expression for average output current and rectification efficiency.
2. Draw the circuit diagram and explain the working of the full wave bridge rectifier and derive the expression for average output current and rectification efficiency.
3. Explain the operation of FWR with center tap transformer. Also derive the following for this transformer (a) DC output voltage, (b) DC output current (c) RMS output voltage. (d) Rectification efficiency.
4. Compare half-wave rectifier, full wave bridge rectifier, and center tap transformer rectifier.
5. Explain the construction and working of Zener diode with a neat sketch.
6. Discuss Zener series regulator.

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## 2.9 FURTHER READINGS

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- Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.
- Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.
- Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.
- Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

## UNIT 3 SPECIAL - PURPOSE DIODES

### NOTES

#### Structure

- 3.0 Introduction
- 3.1 Objectives
- 3.2 Schottky Diode
  - 3.2.1 Difference between the Schottky Diodes and the  $p-n$  Junction Diodes
- 3.3 Tunnel Diodes
- 3.4 Light Emitting Diodes
- 3.5 Answers to Check Your Progress Questions
- 3.6 Summary
- 3.7 Key Words
- 3.8 Self Assessment Questions and Exercises
- 3.9 Further Readings

### 3.0 INTRODUCTION

This unit discusses the different types of special purpose diodes. Special purpose diodes are formed based on different types of doping techniques. Special purpose diodes such as Schottky diodes, tunnel diodes, and light emitting diodes will be discussed in this module. Each type of diodes have a different circuit symbol, different applications and characteristics to be used for special purposes only.

### 3.1 OBJECTIVES

After going through this unit, you will be able to:

- Know about Schottky diode
- Discuss Tunnel diode
- Understand LEDs and their applications.

### 3.2 SCHOTTKY DIODE

A Schottky diode is different from the normal  $p-n$  junction diode in many different ways as discussed below. The Schottky diode has a different circuit symbol as shown in Figure 3.1.



**Fig. 3.1** Schottky Diode Circuit Symbol

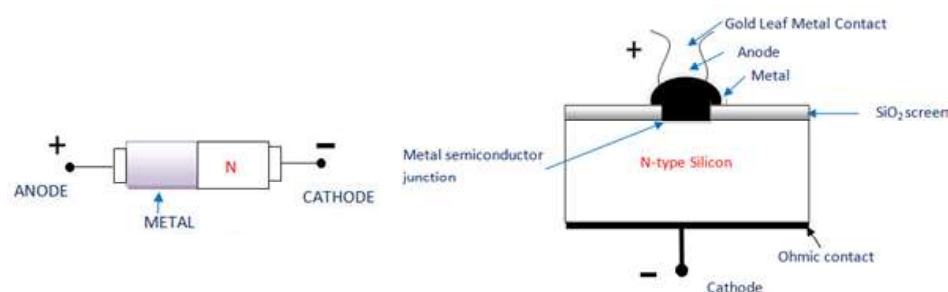


## NOTES

The anode part of the diode is similar to the  $p$ - $n$  junction diode but the cathode of the diodes is “S” shaped representing the Schottky. The main difference between the  $p$ - $n$  junction diode and the Schottky diode is the forward voltage drop ( $V_f$ ) of the  $p$ - $n$  diode is much higher than the Schottky diode. Schottky diodes have a  $V_f$  of around 0.2 volts to 0.5 volts, whereas  $p$ - $n$  junction diodes have a  $V_f$  of 0.6 V to 0.8 V. Since the voltage drop across the diode is very less, the power dissipation in the form of heat is also very less for Schottky diodes when compared to  $p$ - $n$  junction diodes. In Schottky diodes, the conduction is through only one type of charge carriers and hence they are unipolar devices. Unipolar devices are devices in which the current conduction takes place through only one type of charge carriers that is either through electrons or through holes. Schottky diodes are mainly used in SMPS (Switched mode power supply) circuits, due to low temperature rise and high switching speed of the diode between ON and OFF states. The reverse recovery current of Schottky diode is very less compared to any other diodes. When a diode is switched OFF, the time taken by the forward flowing current to die down is called as **reverse recovery time**. The Schottky diode experiences a very short breakdown voltage of around 20 to 40 voltage as against  $\sim 200$ V in a normal  $p$ - $n$  junction diode. With such short breakdown voltages, the Schottky diodes are very much unsuitable for rectifier operation.

## Construction

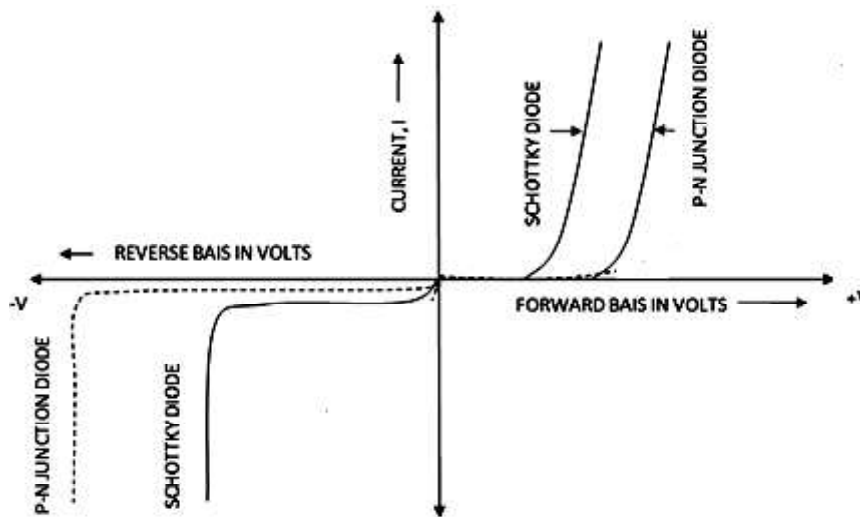
Schottky diodes consist of an  $n$ -type semiconductor and a metal thereby forming a metal-semiconductor junction similar to  $p$ - $n$  junction in normal diodes. In an  $n$ -type semiconductor, the majority carriers are electrons and the majority carriers in a metal are also electrons. The electrons in the  $n$ -type semiconductor exhibit a higher kinetic energy than the electrons on the metal regions. The injected electrons with high kinetic energy from the  $n$ -type to the metal side are called hot carriers. The construction of the Schottky diode is represented in Figure 3.2.



**Fig. 3.2** Schottky Diode

When the  $p$ -type and metal comes into contact, the electrons get injected to the metal side leading to depletion of electrons on the  $n$ -type semiconductor. As more electrons get injected into the metal, an electron wall is created on the metal side. This region is similar to the depletion region of the  $p$ - $n$  diode. In this region with depleted electrons on one side and the electron wall on the other side create a charge-free region. This charge-free region does not hold any charges and hence cannot store any charge during the process of switching from positive to negative and negative to positive input polarity. Such kind of diodes is very much useful for the high-speed switching applications. These diodes can also be used for frequencies ranging around 300 MHz where the switching speed between the polarities is very high. In  $p$ - $n$  junction diodes, when the input voltage frequencies increases, due to the inability of the charge carriers to reverse the direction of flow during the change in the polarity, they exhibit a negative current leading to charge storage inside the depletion region of the  $p$ - $n$  junction diode. This drawback of  $p$ - $n$  junction diode can be avoided using Schottky diodes. The  $v$ - $i$  characteristics of the Schottky diode are given in Figure 3.3. The characteristics of the Schottky diodes in comparison with the  $p$ - $n$  junction diode exhibits a lower breakdown voltage.

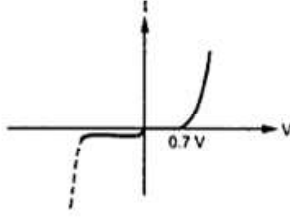
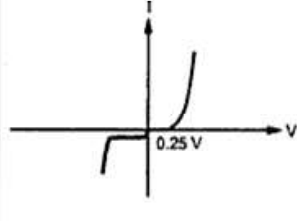


## NOTES



**Fig. 3.3** Characteristics Comparison of Schottky Diode and  $p$ - $n$  Junction Diode

### 3.2.1 Difference between the Schottky Diodes and the $p$ - $n$ Junction Diodes

#### NOTES

Parameter	p-n junction diode	Schottky diode
Junction	Semiconductor to semiconductor	Semiconductor to metal
Carriers	Minority and majority	Only majority
Reverse recovery time	More	Less
Barrier potential	More about 0.7 V	Less about 0.25 V
Breakdown voltage	More	Less
Switching speed	Less	High
PIV rating	More	Less
Frequency range	Upto 10 MHz	Very high more than 300 MHz
Characteristics		
Symbol		

#### Check Your Progress

1. What is the difference between Schottky diode and p-n junction diode?
2. What are unipolar devices?
3. What is reverse recovery time?

### 3.3 TUNNEL DIODES

A tunnel diode is another special purpose diode similar to  $p$ - $n$  junction diode but with the difference in doping. Tunnel diode is exposed to very high doping of the order of 1 part in  $10^3$  impurities. Tunnel diode works on the principle of tunneling. The process of tunneling can be best explained using the energy band diagram of the tunnel diode. The circuit symbol of the tunnel diode is given in Figure 3.4. The anode part of the symbol is similar to the other types of the diode, but the cathode part of the diode resembles the letter "T" of the tunnel.

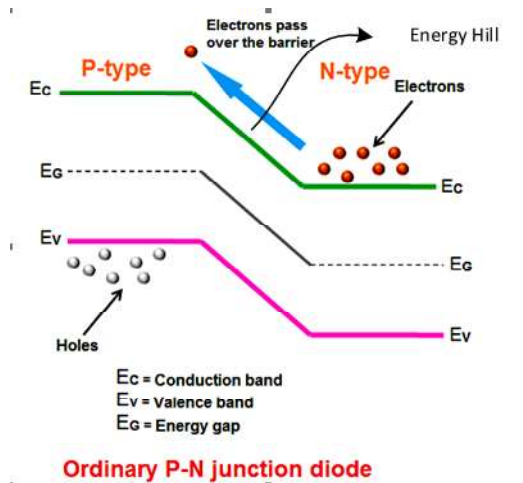


Fig. 3.4 Circuit Symbol of the Tunnel Diode

### Working of the tunnel diode:

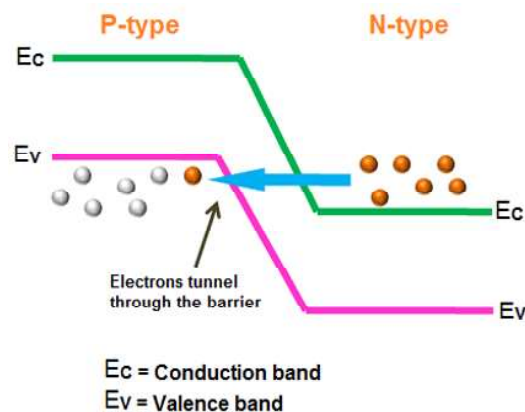
The working of the tunnel diode is explained after a brief working of the normal  $p$ - $n$  junction diode with respect to the energy band diagram as shown in Figure 3.5. During the forward bias of the  $p$ - $n$  junction diode, the electrons in the conduction band of the  $n$ -type material have to overcome the energy barrier or known as electron hill to move to the conduction band of the  $p$ -type material.

### NOTES



**Fig. 3.5** Energy Band Diagram of the  $p$ - $n$  Junction Diode.

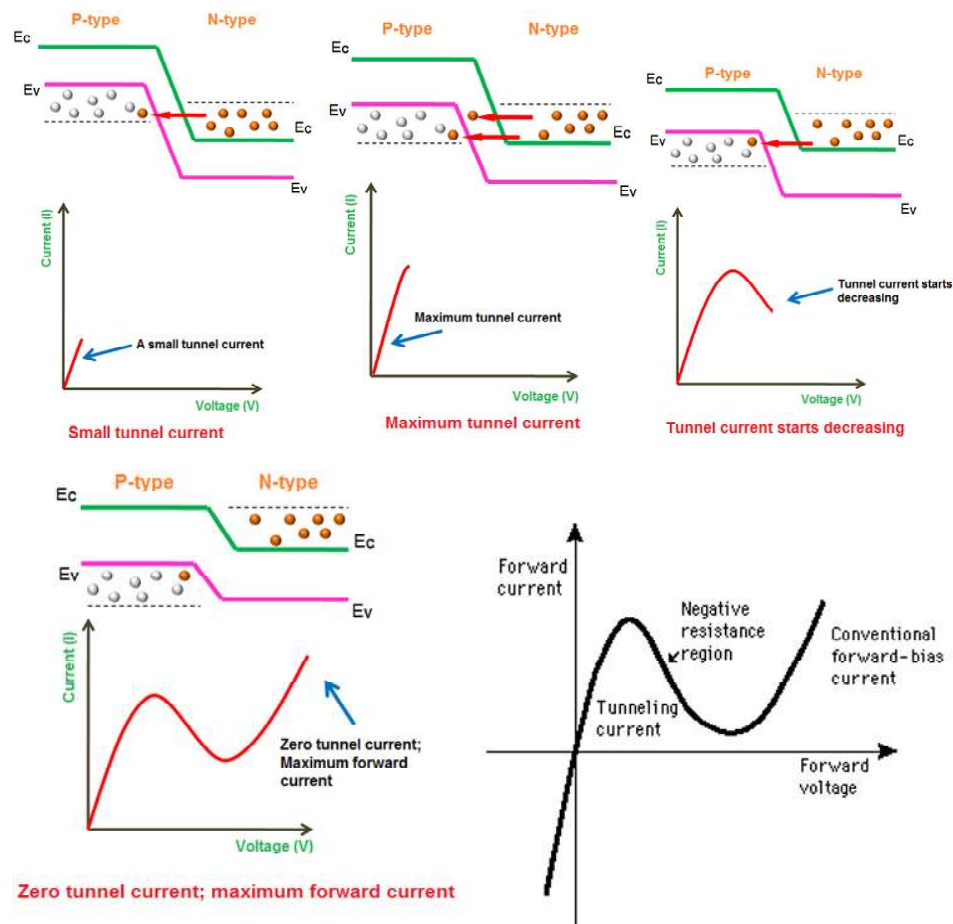
In tunnel diodes, since the diode is heavily doped, the energy level of the  $p$ -side and the  $n$ -side are very different as shown in Figure 3.6. Unlike the conventional diodes, the energy level of the conduction band of the  $n$ -type is in line with the  $p$ -type valence band as shown in Figure 3.6. Also, due to heavy doping, the depletion region is very thin making the energy hill much steeper. When a very low positive voltage is applied, the electrons instead of climbing through the energy hill, it tunnels from the conduction band of the  $n$ -type to the valence band of the  $p$ -type without overcoming the energy hill barrier. The above tunneling effect can also be observed as since the depletion region is very thin and the electrons have a very large energy level, they penetrate the depletion region with ease at a very high velocity.



**Fig. 3.6** Energy Band Diagram of the Tunnel Diode.

## NOTES

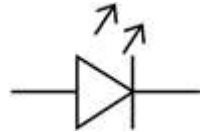
When a slightly positive voltage is applied to the tunnel diode, due to the tunnel effect, the tunnel current increases without any forward conduction current. The characteristics of the tunnel diode is shown in Figure 3.7. When the applied voltage is increased further, the energy level of the  $p$ -type and  $n$ -type side will be at the same level maximizing the tunneling effect. At this moment, maximum tunneling current flows through the diode. On further increasing the applied voltage, the energy level the  $n$ -type semiconductor is much higher than the  $p$ -type side leading to misalignment of both the conduction bands of  $p$  and  $n$ -type sides. This leads to a decrease in the tunneling current. This property of decrease in the tunneling current is an important property of the tunnel diode. Obtaining the slope at this point of the curve provides negative resistance of the diode. On further increasing the applied voltage further, the energy level of the  $n$ -type side rises further leading to complete misalignment for the tunneling process. This makes the tunneling current to zero and the current flows inside the diode similar to the normal  $p$ - $n$  junction diode.



**Fig. 3.7** The Stages of Tunneling Effect in the Tunnel Diode using Energy Band Diagram

### 3.4 LIGHT EMITTING DIODES

Light Emitting Diodes (LEDs) are another common special purpose diodes. The LED emits light when it is forward biased and hence they are optical diodes. The circuit symbol of LED is similar to the  $p$ - $n$  junction diode, except that two arrows pointing outwards from the diode is represented depicting the emission of light rays. The circuit symbol of LED is shown in Figure 3.8.



**Fig. 3.8** Circuit Symbol of Light Emitting Diode (LED)

#### Construction and Working

LED consists of a  $p$ - $n$  junction structure. The majority carriers in  $p$ -type are holes and the majority carriers in  $n$ -type are electrons. When a forward biased voltage is applied, the electrons and the holes recombine. The process of recombination leads to the dissipation of energy by the electrons. The magnitude of the energy released during the process of recombination determines the colour of the light dissipated. When the electrons in the conduction band of  $n$ -type semiconductor, recombine with the hole in the valence band, the release energy equivalent to the band gap energy given as

$$E_g = hf$$

$$= h \left( \frac{c}{\lambda} \right)$$

Where  $h$  = Planck's constant =  $6.62607004 \times 10^{-34}$  m<sup>2</sup> kg/s

$f$  = Frequency (Hz)

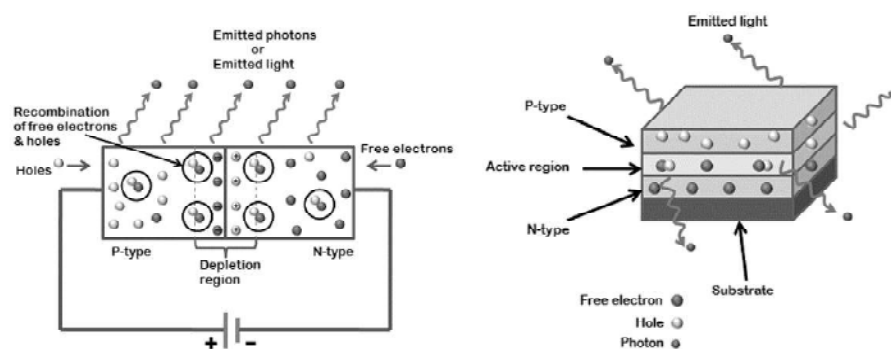
$c$  = Velocity of light (m/s)

$\lambda$  = Wavelength of the light (Å)

When the released energy corresponds to the visible spectrum in the range of 4000 Å to 8000 Å of wavelength, the light rays are produced.

#### NOTES

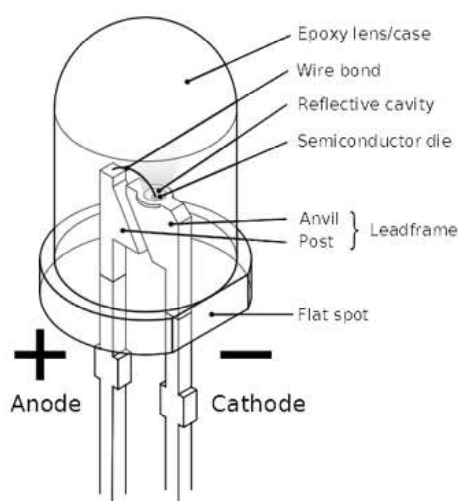
## NOTES



**Fig. 3.9** (a) LED Working (b) Construction

LED consists of three layers of semiconductor that includes a  $p$ -type material,  $n$ -type material and the active region. Active region is equivalent to the depletion region of the  $p$ - $n$  junction diode. The region is said active because the process of recombination and the dissipation of photons takes place primarily in this region of the LED. The given structure in Figure 3.9b consists of photons released in all directions, but the direction of light emission can be focused in a particular direction using the reflectors inside the LEDs.

The practical construction of the LED as shown in Figure 3.10 consists of longer anode terminal and the shorter cathode terminal. The anode terminal is connected to the anvil and the cathode to the post terminal. Anvil and Post are together called as lead frames that establish the contacts. The semiconductor die that consists of  $p$ -type,  $n$ -type and the active region is placed inside a reflective cavity. The reflective cavity is housed in the post of the lead frame. A thin wire strip connects the semiconductor die and the anvil of the anode. The said construction is enclosed in a protective transparent casing such that the light emitted is augmented by the reflector placed inside the LED and the casing prevents from stronger radiation of photons during the forward biasing of the LED.



**Fig. 3.10** Practical LED

## Colours in LED:

Special - Purpose Diodes

The colour light rays dissipated by LEDs depend on the magnitude of the photons released by the electron hole recombination in the active region. The visibility of the radiated light rays is decided based on its wavelength ( $\lambda$ ). Figure 3.11 represents the LED light spectra based on the wavelength. The visible light output for different colours are red is visible at 650 nm, orange at 580 nm, green at 550 nm, blue at 470 nm etc.,

## NOTES

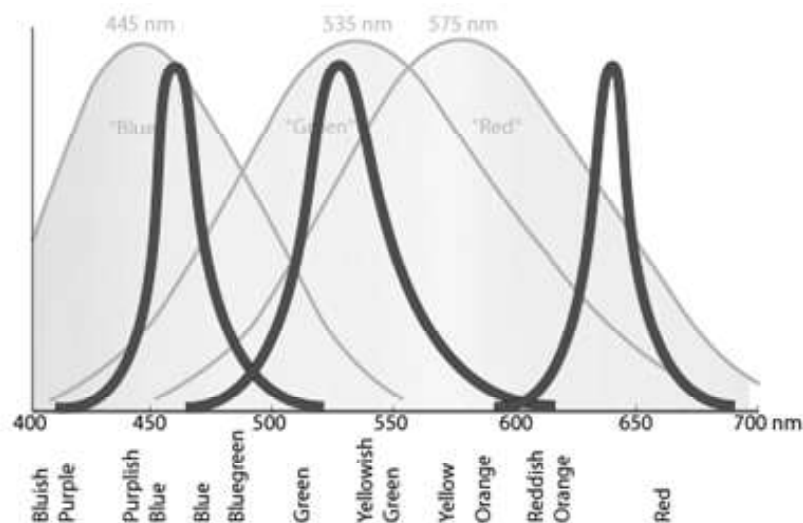


Fig. 3.11 LED Spectra

## Directivity of LEDs

LEDs are highly directional devices. They emit light within  $\pm 15^\circ$  from the center of the main lobe of the light. Reflectors are placed around the LED semiconductor to increase the directivity angle of the visible light. The light radiation pattern is as shown in Figure 3.9. The color spectra of the light can be achieved by proper doping of the  $n$ -type and  $p$ -type materials. Due to unavailability of sophisticated fabrication processes, white LEDs are generated which are encapsulated with the desired colored capsule.

## Types of Light Emitting Diodes

There are different types of light emitting diodes present and some of them are mentioned below.

- Gallium Arsenide (GaAs) – infra-red
- Gallium Arsenide Phosphide (GaAsP) – red to infra-red, orange
- Aluminium Gallium Arsenide Phosphide (AlGaAsP) – high-brightness red, orange-red, orange, and yellow
- Gallium Phosphide (GaP) – red, yellow and green



## NOTES

- Aluminium Gallium Phosphide (AlGaP) – green
- Gallium Nitride (GaN) – green, emerald green
- Gallium Indium Nitride (GaInN) – near ultraviolet, bluish-green and blue
- Silicon Carbide (SiC) – blue as a substrate
- Zinc Selenide (ZnSe) – blue
- Aluminium Gallium Nitride (AlGaIn) – ultraviolet

### Applications of LED

LEDs are used in

- LED is used as a bulb in the homes and industries
- The light emitting diodes are used in the motorcycles and cars
- These are used in the mobile phones to display the message
- At the traffic light signals LEDs are used

### Check Your Progress

4. What are tunnel diodes?
5. What are LEDs?
6. What is the value of Planck's constant?

## 3.5 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

1. The main difference between the  $p$ - $n$  junction diode and the Schottky diode is the forward voltage drop ( $V_f$ ) of the  $p$ - $n$  diode is much higher than the Schottky diode.
2. Unipolar devices are devices in which the current conduction takes place through only one type of charge carriers that is either through electrons or through holes.
3. When a diode is switched OFF, the time taken by the forward flowing current to die down is called as reverse recovery time.
4. A tunnel diode is another special purpose diode similar to  $p$ - $n$  junction diode but with the difference in doping. Tunnel diode is exposed to very high doping of the order of 1 part in  $10^3$  impurities.
5. Light Emitting Diodes (LEDs) are another common special purpose diodes. The LED emits light when it is forward biased and hence they are optical diodes.
6. Planck's constant =  $h = 6.62607004 \times 10^{-34} \text{ m}^2 \text{ kg/s}$

### 3.6 SUMMARY

- The main difference between the  $p$ - $n$  junction diode and the Schottky diode is the forward voltage drop (of the  $p$ - $n$  diode is much higher than the Schottky diode).
- The reverse recovery current of Schottky diode is very less compared to any other diodes. When a diode is switched OFF, the time taken by the forward flowing current to die down is called as reverse recovery time.
- The Schottky diode experiences a very short breakdown voltage of around 20 to 40 voltage as against  $\sim 200\text{V}$  in a normal  $p$ - $n$  junction diode.
- The injected electrons with high kinetic energy from the  $n$ -type to the metal side are called hot carriers.
- A tunnel diode is another special purpose diode similar to  $p$ - $n$  junction diode but with the difference in doping. Tunnel diode is exposed to very high doping of the order of 1 part in impurities. Tunnel diode works on the principle of tunneling.
- Light Emitting Diodes (LEDs) are another common special purpose diodes. The LED emits light when it is forward biased and hence they are optical diodes. The circuit symbol of LED is similar to the  $p$ - $n$  junction diode, except that two arrows pointing outwards from the diode is represented depicting the emission of light rays.

### NOTES

### 3.7 KEY WORDS

- **Diode:** A semiconductor device with two terminals, typically allowing the flow of current in one direction only.
- **Voltage:** An electromotive force or potential difference expressed in volts.
- **Electron:** A stable subatomic particle with a charge of negative electricity, found in all atoms and acting as the primary carrier of electricity in solids.

### 3.8 SELF ASSESSEMENT QUESTIONS AND EXERCISES

#### Short Answer Questions

1. Explain the applications of tunnel diode.
2. What do you mean by negative resistance?
3. Explain the application of Schottky diode.
4. Compare the  $p$ - $n$  junction diode with Schottky diode.
5. Explain the light directivity of LED.

### Long Answer Questions

1. Explain in detail the construction and working of Schottky diode.
2. Explain in detail the construction and working of Tunnel diode.
3. Explain in detail the construction and working of light emitting diode.

### NOTES

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### 3.9 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

**BLOCK - II****TRANSISTOR BIASING AND AMPLIFIER****NOTES****UNIT 4 TRANSISTORS****Structure**

- 4.0 Introduction
- 4.1 Objectives
- 4.2 Construction of BJT
  - 4.2.1 Biasing of BJT
- 4.3 Transistor Operation/Action
  - 4.3.1 Operation of PNP Transistor
  - 4.3.2 Operation of NPN Transistor
  - 4.3.3 Transistor Voltages and Currents
- 4.4 BJT Configurations
  - 4.4.1 Common Base Configuration
  - 4.4.2 Common Emitter Configuration
  - 4.4.3 Common Collector Configuration
- 4.5 Answers to Check Your Progress Questions
- 4.6 Summary
- 4.7 Key Words
- 4.8 Self Assessment Questions and Exercises
- 4.9 Further Readings

**4.0 INTRODUCTION**

In this unit, you will learn about the construction, operation and configurations of transistor. The transistor is a three-layer semiconductor device consisting of either two N-type and one P-type layers of material or two P-type and one N-type layers of the material. The former is called an NPN transistor while the latter is called a PNP transistor. Transistors are also called Bipolar Junction Transistors (BJTs). In transistors, the conduction of current is due to both majority and minority carriers, and hence they are called as bipolar junction transistors. BJTs are current controlled devices. The different working configurations of the transistor, such as CB, CC and CE configurations will be explained in this unit.

**4.1 OBJECTIVES**

After going through this unit, you will be able to:

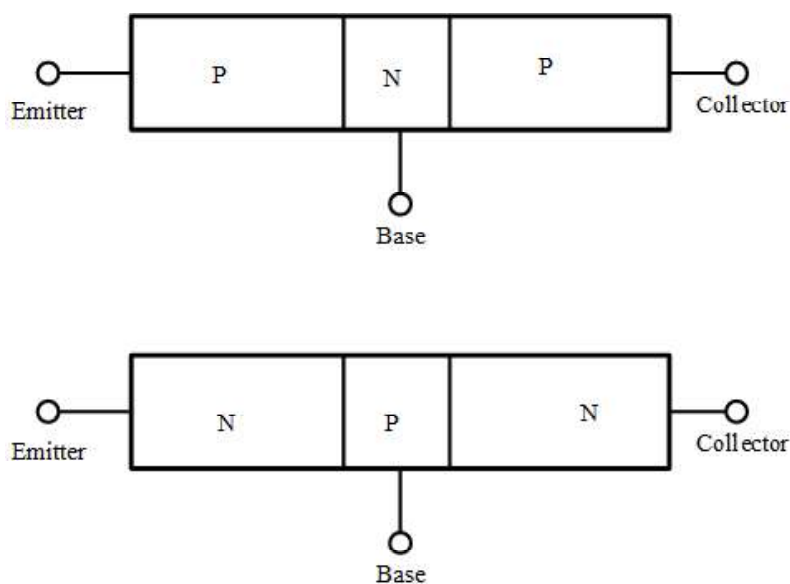
- Explain the construction of BJT
- Understand the operation of NPN and PNP transistor
- Explain the input, output and gain characteristics in CB, CE and CC configurations of a transistor

## 4.2 CONSTRUCTION OF BJT

### NOTES

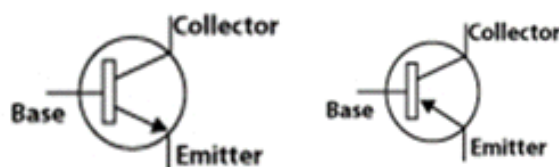
Transistors are constructed from the PN junction diode which have been discussed in the previous units. When an additional P-type material is sandwiched with the PN junction diode, PNP transistor is formed and if the N-type material is sandwiched with P-side of the PN junction diode, NPN transistor is formed. Therefore, PNP transistors consist of two p-type material and one n-type material, NPN transistors consists of two n-type material and one p-type material.

Transistors have three terminals known as an emitter, base, and the collector. The input terminal is called as an Emitter (E) and the output terminal is called as a Collector (C). The third terminal which is the output of the center sandwiched semiconductor is known as a Base (B). The terminal that emits the majority carriers is called as emitters and the one that collects the majority carriers are called as a collector. The structure of the transistors is given in Figure 4.1.



**Fig. 4.1** Transistor Structure

The circuit symbol of the transistors is shown in Figure 4.2. For PNP transistors, the circuit symbol consists of an arrow pointing outwards the emitter terminal. The arrow in the circuit symbol of the transistors represents the flow of electrons. From the structure of the transistors, it is evident that there exist two junctions for both the PNP and NPN transistors. In general, there exists an emitter-base junction and a base-collector junction.



**Fig. 4.2** Transistor Circuit Symbol

The thickness of the base is usually kept small in comparison to the emitter and the collector section of the transistors.

### Currents in the Transistors

There exist three currents in the transistors, they are emitter current  $I_E$ , base current,  $I_B$ , and the collector current,  $I_C$ . The relation between these currents is given below:

$$I_E = I_B + I_C$$

Normally, the base current is always small, such that base current can be ignored. Therefore

$$I_E \approx I_C$$

#### 4.2.1 Biasing of BJT

The emitter-base junction is represented as junction  $J_{EB}$  and the base collector junction is represented as  $J_{BC}$ . Based on the biasing of the junctions  $J_{EB}$  and  $J_{BC}$ , transistors can be used as amplifier or as a switch in ON and OFF condition. The table below gives the required biasing of junctions to achieve the desired applications.

Application	$J_{EB}$	$J_{BC}$
Amplifier	Forward bias	Reverse bias
Switch in ON condition	Forward bias	Forward bias
Switch in OFF condition	Reverse bias	Reverse bias

#### Check Your Progress

1. What is a transistor?
2. What are the two types of transistor?

## NOTES

### 4.3 TRANSISTOR OPERATION/ACTION

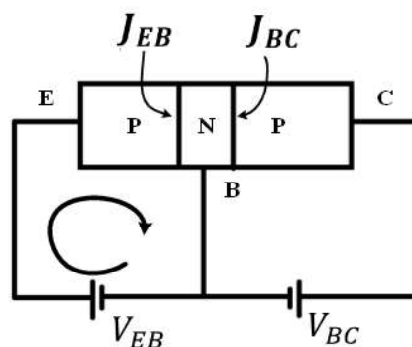
In this section, you will learn about the operation of PNP and NPN transistor.

#### NOTES

#### 4.3.1 Operation of PNP Transistor

The biased PNP transistor is shown in Figure 4.3. Junction  $J_{EB}$  is forward biased and the junction  $J_{BC}$  is reverse biased. The P and N side of the PNP transistor is forward biased. The PN side of the PNP is similar to the PN junction diode and exhibit the forward bias characteristics of the diode. The positive terminal of the voltage  $V_{EB}$  injects more holes to the P type. The holes pass through the junction  $J_{EB}$  easily and recombines with the holes. The majority carriers flows from emitter to P type semiconductor and then to N-type semiconductor through the junction . The majority carriers are holes for the PN side of the transistor. Therefore, holes move from P to N type semiconductors.

The N and P side of the semiconductors are reverse biased by the voltage . When the base collector junction is reverse biased, the minority carriers are holes and the majority carriers are electrons. Since the base terminal is small and are lightly doped, the holes injected from emitter to the P side crosses junction with ease due to forward biasing of the junction . The entered holes have fewer number of electrons to recombine and pass through the junction with ease since holes are the minority carriers in the NP side of the PNP transistor.



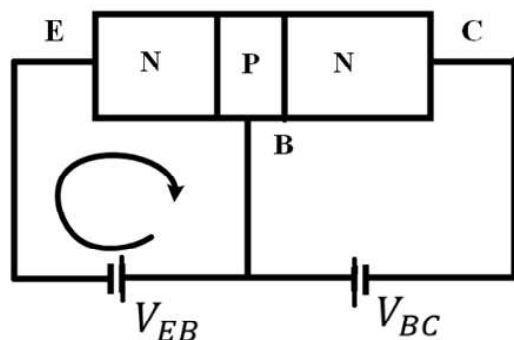
**Fig. 4.3** PNP Transistor Biasing

#### 4.3.2 Operation of NPN Transistor

The biased NPN transistor is shown in Figure 4.4. Junction  $J_{EB}$  is forward biased and the junction  $J_{BC}$  is reverse biased. The N and P side of the NPN transistor is forward biased. The NP side of the NPN is similar to the PN junction diode and exhibit the forward bias characteristics of the diode. The majority carriers flows from emitter terminal to N type semiconductor and then to P-type semiconductor through the junction . The majority carriers are electrons for the NP side of the transistor. Therefore, electrons move from N to P type semiconductors.

The P and N side of the semiconductors are reverse biased by the voltage. When the base collector junction is reverse biased, the minority carriers are electrons and the majority carriers are holes. Since the base terminal is small and are lightly doped, the electrons injected from emitter to the N side crosses junction with ease due to forward biasing of the junction. The entered electrons have fewer number of holes in the P type semiconductor to recombine and pass through the junction with ease since electrons are the minority carriers in the PN side of the NPN transistor.

## NOTES



**Fig. 4.4** NPN Transistor Biasing

### 4.3.3 Transistor Voltages and Currents

The direction of current across the PNP and NPN transistor changes due to the change in majority carriers. Since the flow of holes is considered as the conventional flow of current, in PNP transistors holes flow from emitter to collector. Figure 4.5(a) represents the current direction for PNP transistors where emitter current flows inwards to the circuit and the base current and the collector current flows outwards. The emitter current inside the PNP transistors is given as:

$$I_E = I_B + I_C$$

In NPN transistors, since the conventional current direction is opposite to the electron flow direction, compared to the PNP transistors, the current directions across the emitter, base and the collector terminals are opposite. Across the emitter terminal, the current flows outwards and across the base and the collector terminal, the current flows inwards inside the transistor.

The transistor voltages for both PNP and NPN transistors include the following:

$V_{BE}$  = the base emitter voltage

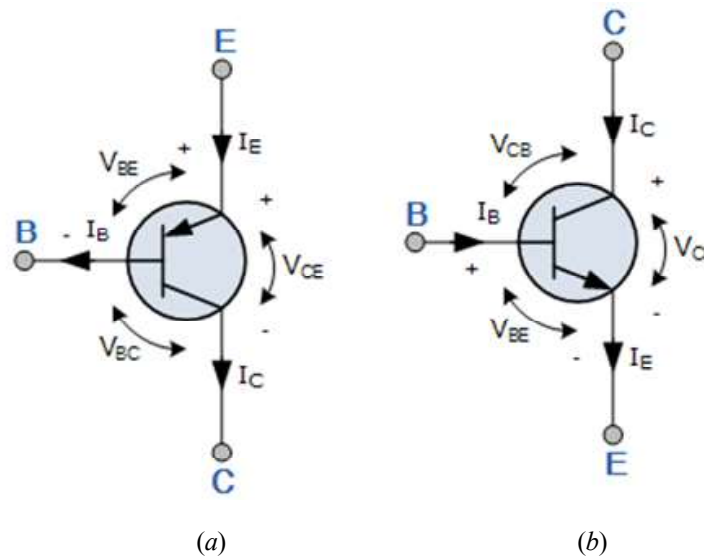
$V_{BC}$  = the base collector voltage

$V_{CE}$  = the collector emitter voltage

$$V_{BC} = V_{BE} - V_{CE}$$



## NOTES



**Fig. 4.5** Transistor Voltages and Currents (a) PNP, (b) NPN

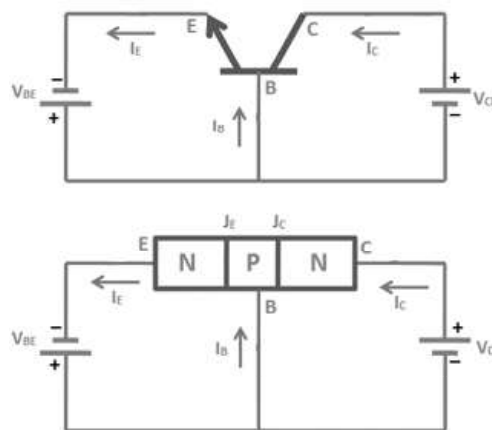
## 4.4 BJT CONFIGURATIONS

Based on the common terminal connected to the two voltage potentials, the working of BJTs can be classified into three configurations.

1. Common Base (CB) configuration
2. Common Emitter (CE) configuration
3. Common Collector (CC) configuration

### 4.4.1 Common Base Configuration

Common base configuration consists of base terminal as the common terminal connected to ground with emitter terminal as an input terminal and the collector as the output terminal. Common base configuration is given in Figure 4.6.



**Fig. 4.6** Common Base Configuration of BJT

The input voltage is the base-emitter voltage,  $V_{BE}$  through a current limiting resistor,  $R_E$ . The base terminal is connected as a common terminal. Base emitter junction is forward biased and the base collector junction is reverse biased. The given BJT is a PNP transistor which is evident from the arrow inside the circuit symbol of the transistor. The load resistor  $R_L$  is connected at the output collector terminal.

There are two types of characteristics associated each type of configuration of transistors. They are

1. Input characteristics
2. Output characteristics

Input characteristics are plotted between the input voltage and input current for that particular configuration and similarly, the output characteristics are plotted between the output voltage and output current for that particular configuration.

### Input Characteristics of CB Configuration

The input voltage for the common base configuration  $V_{BE}$  is and the input current is the emitter current  $I_E$ . Input characteristics is plotted between  $V_{BE}$  and  $I_E$ . Since the voltage is an independent parameter and the current  $I_E$  is dependent on the input voltage, voltage  $V_{BE}$  will be on x-axis and the current will be on the y-axis. Since the PN semiconductor of PNP transistor is similar to the PN junction diode, the input characteristics will be similar to the diode characteristics. The input characteristics is plotted by varying the input voltage  $V_{BE}$  with fixed  $V_{CB}$  voltages starting from zero volts. As the  $V_{CB}$  voltages is increased, the reverse biased junction  $J_{BC}$  has more number of electrons to recombine with the incoming holes through the emitter and hence the flow of electrons from the emitter to the base junction is faster. Hence, the input characteristics shows earlier conduction of current as  $V_{CB}$  voltage is increased.

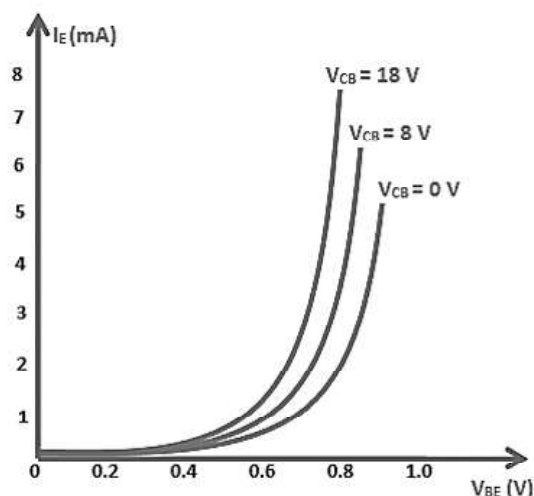


Fig. 4.7 Input Characteristics of CB Configuration of BJT

## NOTES

## NOTES

**Output Characteristics of CB Configuration of BJT**

The output voltage of the CB configuration of the BJT is  $V_{CB}$  and the output current is  $I_C$ . The output characteristics is plotted between  $V_{CB}$  and  $I_C$  with the fixed input voltage  $V_{EB}$ . Collector current  $I_C$  depends on the applied output voltage  $V_{CB}$  and hence,  $I_C$  is a dependent current and  $V_{CB}$  is an independent voltage. The output characteristics for CB configuration is plotted in Figure 4.8. As  $V_{EB}$  is varied, the input current  $I_E$  also varies and hence the controlling parameter is the emitter current,  $I_E$ . Observing from the characteristics for  $I_E = 0$ , implies that there exists no input voltage, leading to no biasing of the junction  $J_{EB}$  and hence no input current. When there exists no input current, there will be no current flow in the transistor and hence the characteristics depicts  $I_C = 0$  (mA) current. As input voltage and in turn the input emitter current is increased, the collector current increases equivalently. Since the base current,  $I_B$  is approximately zero, the collector current is equal to the emitter current i.e.  $I_E \approx I_C$ . Also, as observed from the characteristics, when a negative output voltage,  $V_{CB}$  is applied across the junction  $J_{BC}$ , the said junction is forward biased and augments for the flow of collector current. And hence, as is shown from Figure 4.8, for a negative output voltage, the collector current increases and stays at a constant value when  $V_{CB} = 0V$ .

Output characteristics shows three regions of operation. They are

1. Saturation region
2. Cut off region and
3. Active region

For the application of transistors as a switch in an ON condition, the transistor is made to operate in the saturation region, for application as a switch in an OFF condition, the transistor is made to operate in the cut-off region. For use of transistors as amplifiers, they are made to operate in the active region.

Saturation region is the region of operation of the transistor, where the output applied voltage is zero, but there exists collector current dependent on the input emitter current,  $I_E$ . This region is similar to the switch in an ON condition or a short circuited condition of a circuit.

In the cutoff region, there exists no collector current for any change in voltage. Voltage, just reverse biases the junction, . Without any input current, , the collector current is zero. This condition is very well used as a switch in the OFF condition.

The active region comprises of the limits,  $V_{CB} > 0$ ,  $I_E > 0$  and  $I_C > 0$ . this is the region that is used to operate transistor as amplifiers. The detailed working of the transistor as amplifier will be dealt in the subsequent unit under power amplifiers.

The biasing conditions for the three configurations are given in the table below:

Table 4.1 Biasing condition and application of BJT.

Transistors

Region of operation	Emitter-base junction, $J_{EB}$	Base-collector junction, $J_{BC}$	Application
Saturation region	Forward Biased	Forward Biased	Switch in ON mode
Cut off region	Reverse Biased	Reverse Biased	Switch in OFF mode
Active region	Forward Biased	Reverse Biased	Amplifier

NOTES

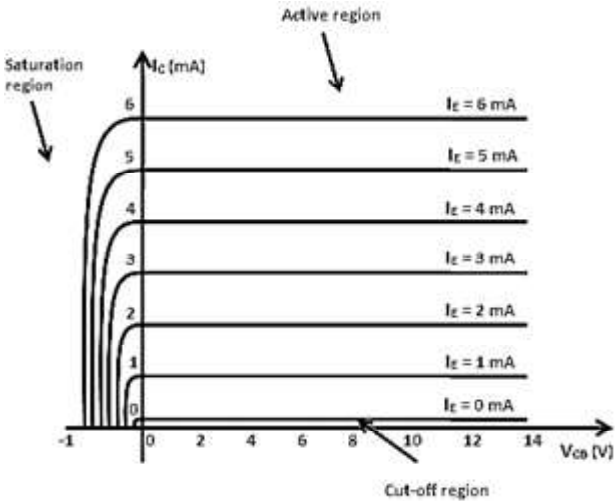


Fig. 4.8 Output Characteristics of CB Configuration of BJT

Current Gain

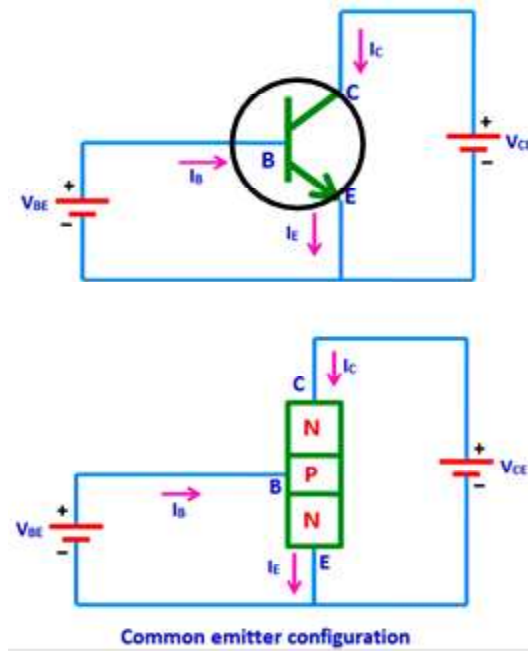
The gain for a CB configuration is the ratio of output collector current,  $I_C$  and the input emitter current,  $I_E$ . The gain is represented as,

$$\alpha = \frac{I_C}{I_E}$$

4.4.2 Common Emitter Configuration

In common emitter configuration, the emitter is common to both the base and the collector terminal. Base terminal is considered the input terminal and the collector terminal is the output terminal. Similar to the CB configuration of BJT, the input and output characteristics are given below.

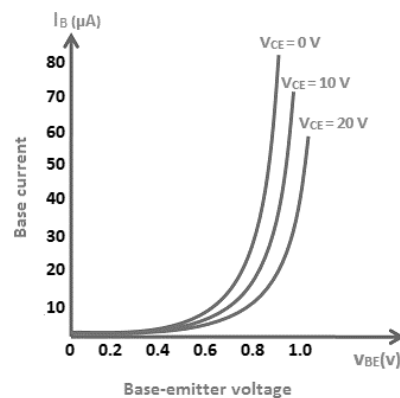
## NOTES



**Fig. 4.9** Common Emitter (CE) Configuration of BJT

### Input Characteristics

The input characteristics are plotted between the input voltage  $V_{BE}$  and input current  $I_B$ . The n and P regions are forward biased in the PNP transistor. Hence the current flows from  $I_B$  to  $I_E$  in the absence of a collector terminal or with open circuited collector terminal. The input characteristics follows a diode characteristics. The base current rises after the cutin voltage with an increase in  $V_{BE}$ . As the reverse biased  $V_{CE}$  is increased, the junction  $J_{BC}$  is more reverse biased obstructing the flow of input current to the output terminals. Hence, the input characteristics shifts towards the right for an increase in  $V_{CE}$  as shown in Figure 4.10.



**Fig. 4.10** Input Characteristics of CE Configuration of BJT

## Output Characteristics of CE Configuration of BJT

The output characteristics are plotted between the output voltage  $V_{CE}$  and the output current,  $I_C$  for fixed input current,  $I_B$ . The input base current can be controlled by the input voltage,  $V_{BE}$ . When input current  $I_B = 0$ , then there exists no output current. The corresponding region is highlighted in the output characteristics as **cutoff region**.

For a fixed input current of  $I_B$ , as the reverse biased junction is increased aiding the minority carriers to flow, the output collector current, equivalent to the emitter current flows in the circuit. It is to be observed that since the base region is lightly doped, the base current flows of the order of microamperes, whereas the emitter current and collector current of the order of milliamperes. The region corresponding to  $V_{CE} > 0$ ,  $I_B > 0$  and  $I_C > 0$  is the active region of the BJT.

With the control voltage  $V_{CE} = 0$  V, with an increase in the input base current,  $I_B$ , the collector current increases as shown in Figure 4.11. The collector current will be equal to the emitter current with base current as the controlling current. The working of the transistor in CE configuration may be viewed as a switch with a controlling input in the form of base current,  $I_B$ . The magnitude of the current from emitter to collector is controlled by  $I_B$ . It is similar to the water tap analogy, where the control knob controls the flow of water from the tap to the outlet.

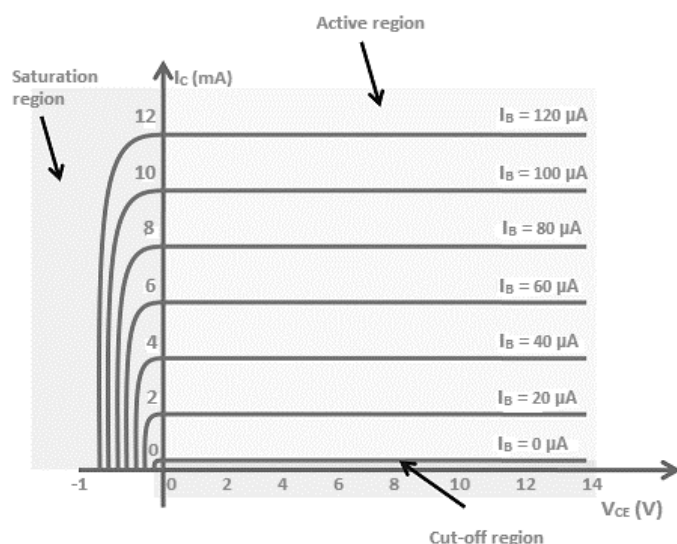


Fig. 4.11 Output Characteristics of CE Configuration of BJT

## Current Gain

The gain of the CE configuration is denoted as  $\beta$ . The current gain is the ratio of the output current,  $I_C$  and the input current  $I_B$ . Mathematically, it is given as

$$\beta = \frac{I_C}{I_B}$$

## NOTES

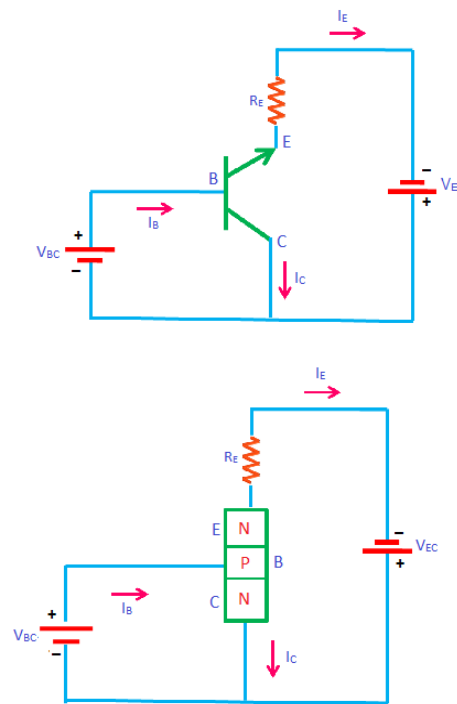
The above expression can also be rewritten as

$$I_C = \beta I_B$$

## NOTES

### 4.4.3 Common Collector Configuration

In common collector configuration, the collector terminal is the common terminal and the base terminal is the input terminal and the emitter is the output terminal. The base-collector junction is forward biased and the base-emitter junction is reverse biased. The input current is the base current and the output current is the emitter current. Such configuration is widely used as a voltage buffer. The input voltage to the CC configuration is base-collector voltage,  $V_{BC}$  and the output voltage is emitter collector voltage,  $V_{EC}$ . The common collector amplifier has high input impedance and low output impedance. It has low voltage gain and high current gain. The common collector configuration is shown in Figure 4.12.



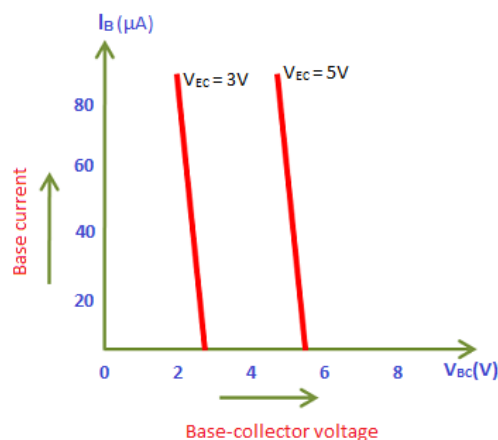
**Fig. 4.12** Common Collector (CC) Configuration of BJT

### Input Characteristics for CC Configuration

The input characteristics of common collector configuration are plotted between the input base-collector voltage,  $V_{BC}$  and the input base current  $I_B$  for a fixed output emitter collector voltage,  $V_{EC}$ . The independent parameter,  $V_{BC}$  is drawn on the x-axis and the dependent parameter,  $I_B$  is plotted on the y-axis. For a fixed value of  $V_{EC}$  voltage, the  $V_{BC}$  voltage is varied and the base current is plotted. The characteristics as shown in Figure 4.13, the emitter and the collector terminals are tied by the applied  $V_{EC}$  voltage. The emitter terminal is at higher polarity than the

collector terminal. As the input voltage,  $V_{BC}$  is applied to the base-collector junction, it forward biases the junction and conduction starts instantly at the cut in voltage. As the  $V_{BC}$  voltage is increased further, it has to overcome the emitter collector potential. When both the potentials are equal, net potential across the transistor is zero and no current takes place. It is evident from the input characteristics that for  $V_{EC} = 3V$ , when  $V_{BC} = 3V$ , the input current becomes zero. Similarly for the other fixed voltage of  $V_{EC} = 5V$ , current conduction stops when the input voltage  $V_{BC} = 5V$ .

## NOTES



**Fig. 4.13** Input Characteristics of Common Collector (CC) Configuration of BJT

## Output Characteristics of CC Configuration

The output characteristics are plotted between the output emitter-collector voltage,  $V_{EC}$  and emitter current,  $I_E$  for fixed input base currents,  $I_B$ . For a fixed value  $I_B$ , the voltage,  $V_{EC}$  is varied along x-axis and  $I_E$  is plotted along the y-axis. Similar to the other configurations, there exists the active region, cut-off region and the saturation region.

It is to be noted that, the emitter terminal and the collector terminals can be used interchangeably. Therefore, CE and CC configuration exhibit similar working characteristics. The cut-off region is the operating region where the emitter current,  $I_E = 0$  for any change in voltage,  $V_{EC}$  for a fixed base current,  $I_B = 0$ . As the base current is increased, the conduction path between the emitter and the collector is established. The working is similar to the water tap analogy, where the controlling knob is equivalent to the base current and the water flow from tap to the outlet can be related to the current flowing from collector terminal to the emitter terminal.

The saturation region is the region where for  $V_{EC} = 0$ , there exists an emitter current,  $I_E$ . The larger the magnitude of the base current, the larger is the magnitude of emitter current as is evident from the output characteristics.

Active region comprises of  $I_E > 0$ ,  $V_{EC} > 0$  and  $I_B > 0$ . This is the region used for amplification purposes.



## NOTES

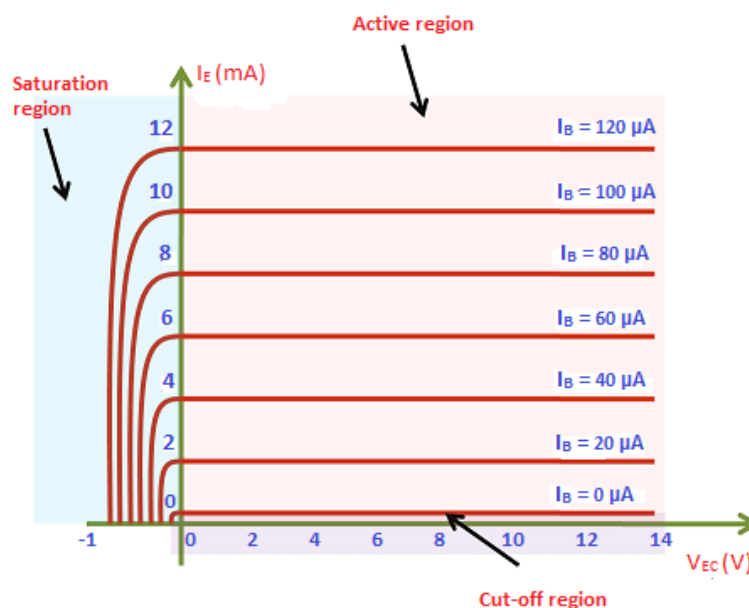


Fig. 4.14 Output Characteristics of CC Configuration of BJT

### Current Gain

The gain in the common collector configuration is denoted as  $\gamma$ . The current gain is given as the ratio of the output emitter current,  $I_E$  to the input base current,  $I_B$ . Mathematically it is represented as:

$$\gamma = \frac{I_E}{I_B}$$

### Relations between $\alpha$ and $\beta$

We know that,

$$\alpha = \frac{I_C}{I_E} \Rightarrow I_E = \frac{I_C}{\alpha}$$

and

$$\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$$

Also,

$$I_E = I_B + I_C$$

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\alpha = \frac{\beta}{1 + \beta}$$

The above expression is current gain,  $\alpha$  in terms of  $\beta$

$$I_E = I_B + I_C$$

$$\frac{I_C}{\alpha} = \frac{I_C}{\beta} + I_C$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} - 1 = \frac{1}{\beta}$$

$$\frac{1 - \alpha}{\alpha} = \frac{1}{\beta}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

### Relations between $\alpha$ , $\beta$ and $\gamma$

We know that,

$$\gamma = \frac{I_E}{I_B} \Rightarrow I_E = \gamma I_B$$

$$\beta = \frac{I_C}{I_B} \Rightarrow I_C = \beta I_B$$

$$I_E = I_B + I_C$$

$$\gamma I_B = I_B + \beta I_B$$

$$\gamma = 1 + \beta$$

The above expression is  $\gamma$  in terms of  $\beta$ . Similarly,  $\gamma$  in terms of  $\beta$  is given as,

We know that,

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\gamma = 1 + \beta \Rightarrow \beta = \gamma - 1$$

$$\gamma = 1 + \frac{\alpha}{1 - \alpha} = \frac{1 - \alpha + \alpha}{1 - \alpha}$$

$$\gamma = \frac{1}{1 - \alpha}$$

$$1 - \alpha = \frac{1}{\gamma}$$

### NOTES

**NOTES**

$$\alpha = 1 - \frac{1}{\gamma}$$

$$\alpha = \frac{\gamma - 1}{\gamma}$$

Summary of relationships between  $\alpha$ ,  $\beta$  and  $\gamma$ :

$$\beta = \frac{\alpha}{1 - \alpha}$$

$$\alpha = \frac{\beta}{1 + \beta}$$

$$\gamma = 1 + \beta$$

$$\beta = \gamma - 1$$

$$\alpha = \frac{\gamma - 1}{\gamma}$$

$$\gamma = \frac{1}{1 - \alpha}$$

**Table 4.2** Comparison of CB, CE and CC configuration.

Characteristics	CB	CE	CC
Input Resistance	low (about 100 $\Omega$ )	Medium (800 $\Omega$ to few K $\Omega$ )	High (about 750k $\Omega$ )
Output Resistance	Very High (about 500k $\Omega$ )	High (about 50k $\Omega$ )	Low (about 50 $\Omega$ )
Input Current	$I_E$	$I_B$	$I_B$
Output Current	$I_C$	$I_C$	$I_E$
Input Voltage applied between	E & B	B & E	B & C
O/p Voltage taken between	C & B	C & E	E & C
Current gain	$\alpha = I_C/I_E$ (less than unity, 0.95 to 0.99)	$\beta = I_C/I_B$ (High, 25 to 400)	$\gamma = I_E/I_B$ (High)
Voltage gain	About 150	About 500	Less than unity
Power gain	Medium	High	Medium
Output Signal phase	In phase with the input	Reverse ( $180^\circ$ )	In phase with the input
Application	For high-Frequency Circuits	For Audio Frequency Circuits	For impedance matching
Common Terminal	Base	Emitter	Collector
Leakage Current	Very Small	Very Large	Very Large

**Check Your Progress**

3. What are the different types of working configuration of BJT?
4. Write the relation between  $\alpha$  and  $\beta$ .

**NOTES**

## 4.5 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

1. The transistor is a three-layer semiconductor device consisting of either two N-type and one P-type layers of material or two P-type and one N-type layers of the material.
2. NPN and PNP are the two types of transistors.
3. The working of BJTs can be classified into three configurations.
  - (i) Common Base (CB) configuration
  - (ii) Common Emitter (CE) configuration
  - (iii) Common Collector (CC) configuration
4. The relation between  $\alpha$  and  $\beta$  is given below.

$$\alpha = \frac{\beta}{1 + \beta}$$

## 4.6 SUMMARY

- The transistor is a three-layer semiconductor device consisting of either two N-type and one P-type layers of material or two P-type and one N-type layers of the material. The former is called an npn transistor while the latter is called a PNP transistor.
- When an additional P-type material is sandwiched with the PN junction diode, PNP transistor is formed and if the N-type material is sandwiched with P-side of the PN junction diode, NPN transistor is formed.
- Transistors have three terminals known as an emitter, base, and the collector. The input terminal is called as an Emitter (E) and the output terminal is called as a Collector (C). The third terminal which is the output of the center sandwiched semiconductor is known as a Base (B).
- There exist three currents in the transistors, they are emitter current  $I_E$ , base current,  $I_B$ , and the collector current,  $I_C$ .
- The direction of current across the PNP and NPN transistor changes due to the change in majority carriers.

## NOTES

- The emitter current inside the PNP transistors is given as:

$$I_E = I_B + I_C$$

- The working of BJTs can be classified into three configurations i.e. Common Base (CB) configuration, Common Emitter (CE) configuration and Common Collector (CC) configuration.
- Common base configuration consists of base terminal as the common terminal connected to ground with emitter terminal as an input terminal and the collector as the output terminal.
- Input characteristics are plotted between the input voltage and input current for that particular configuration and similarly, the output characteristics are plotted between the output voltage and output current for that particular configuration.
- In common emitter configuration, the emitter is common to both the base and the collector terminal. Base terminal is considered the input terminal and the collector terminal is the output terminal.
- In common collector configuration, the collector terminal is the common terminal and the base terminal is the input terminal and the emitter is the output terminal.

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#### 4.7 KEY WORDS

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- **Emitter (E):** It is the region to the left end which supply free charge carriers, i.e., electrons in  $n-p-n$  or holes in  $p-n-p$  transistor and these majority carriers are injected to the middle region.
  - **Base (B):** It is the middle region where either two P-type layers or two  $n$ -type layers are sandwiched.
  - **Collector (C):** It is the region to the right end where charge carriers are collected.
- 

#### 4.8 SELF ASSESSMENT QUESTIONS AND EXERCISES

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##### Short Answer Questions

1. Why are common base type materials lightly doped?
2. How are PNP or NPN transistors formed?
3. What is the biasing requirement for operating transistor as an amplifier?
4. What is the biasing requirement for operating transistor as a switch?
5. Compare the relation between current gains,  $\alpha$ ,  $\beta$  and  $\gamma$ .

6. Compare the different configuration of BJT.
7. Draw the common base configuration of BJT.
8. Draw the common emitter configuration of BJT.
9. Draw the common collector configuration of BJT.
10. Draw the input-output characteristics of CB configuration of BJT
11. Draw the input-output characteristics of CE configuration of BJT
12. Draw the input-output characteristics of CC configuration of BJT
13. What are the different regions of operation of BJT?
14. Discuss the importance of operation of the active region.
15. Describe the current relation inside BJT.

## NOTES

### Long Answer Questions

1. Explain the construction and working of common emitter configuration for PNP transistor.
2. Explain the construction and working of common base configuration for PNP transistor.
3. Explain the construction and working of common collector configuration for the PNP transistor.
4. Derive the relation between the current gains  $\alpha$ ,  $\beta$  and  $\gamma$ .

## 4.9 FURTHER READINGS

- Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.
- Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.
- Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.
- Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

## UNIT 5 TRANSISTOR AMPLIFIER

### NOTES

#### Structure

- 5.0 Introduction
- 5.1 Objectives
- 5.2 Application of Transistor
  - 5.2.1 Load Lines
  - 5.2.2 Small Signal Analysis of the Amplifiers
  - 5.2.3 Hybrid Equivalent Circuits of Two Port Networks
  - 5.2.4 Small Signal Amplifier Analysis using H Parameters - General Model
- 5.3 Power Amplifiers
  - 5.3.1 Class A Amplifier
  - 5.3.2 Class B Amplifier
  - 5.3.3 Class AB Amplifier
  - 5.3.4 Class C Amplifier
- 5.4 Answers to Check Your Progress Questions
- 5.5 Summary
- 5.6 Key Words
- 5.7 Self Assessment Questions and Exercises
- 5.8 Further Readings

### 5.0 INTRODUCTION

In this unit, you will learn about the use of transistors as an amplification device and the methods of analyzing the amplifiers using equivalent circuits. Transistors operate in three modes i.e. as an amplifier when they operate in the active region, as a switch in ON state when they operate in the saturation region and as a switch in OFF state when they operate in the cut-off region. Analysis of the transistor amplifier using the equivalent circuit to determine the input impedance, output impedance, current gain, voltage gain, bandwidth product will also be discussed in this unit.

Further, you will also learn about the operation of different power amplifiers such as class A, class B, and class C amplifiers. *Power amplifier* is an electronic amplifier designed to increase the magnitude of power of a given input signal.

### 5.1 OBJECTIVES

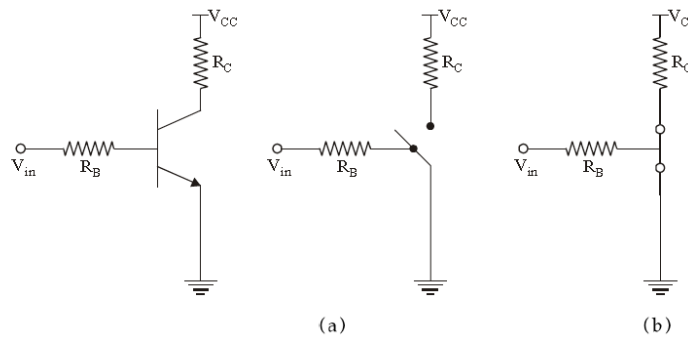
After going through this unit, you will be able to:

- Discuss the applications of transistor
- Define power amplifier
- Explain the different types of power amplifier along with their input-output characteristics
- Discuss the characteristics of power amplifier

## 5.2 APPLICATION OF TRANSISTOR

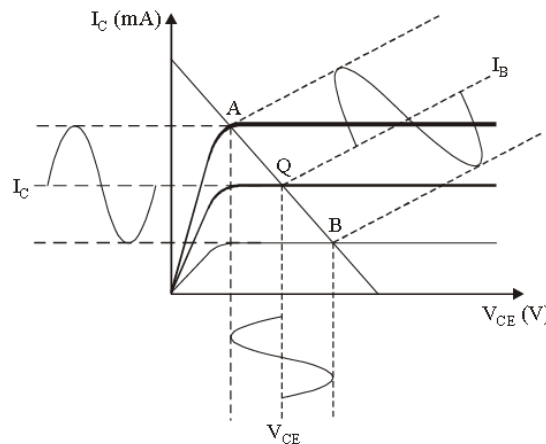
Bipolar junction transistors (BJTs) are generally used as amplifiers, switch in an open condition and switch in a closed condition. The output characteristics of a transistor consist of three regions. Three regions include an active region, saturation region and cut off region. When a transistor is operated in the active region, they operate as amplifiers, when a transistor operates in the saturation region, they operate as a switch in an open circuit and when a transistor operates in the cut-off region, and they operate as a switch in a closed circuit. Figure 5.1 shows the equivalent circuit of a transistor when it operates in saturation and cut off regions.

### NOTES



**Fig. 5.1** The Equivalent Circuit of the Transistor while Operating in (a) Cut Off (b) Saturation

The process of amplification is illustrated in Figure 5.2. When the input signal is within the active region, proper amplification takes place. The signal gets distorted when a part of the input signal reaches the cut-off or saturation region.



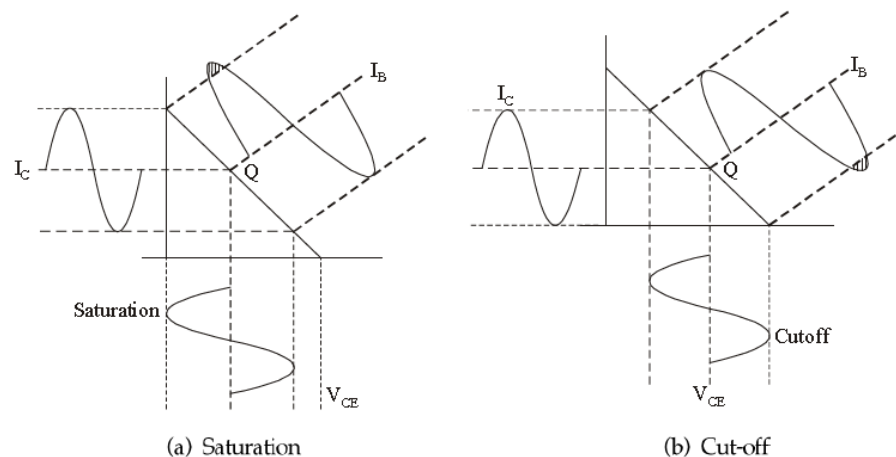
**Fig. 5.2** Transistor Amplification using Output Characteristics

In Figure 5.3 (a) the input signal,  $I_E$  varies in the active region and a portion of the positive cycle, reaches the saturation region. During this section of the cycle, the transistor is driven to saturation and act as a switch in an open circuit. This results in the output voltage  $V_{CE}$  and output current  $I_C$  to have a clipped signal on



## NOTES

the positive cycle as shown in Figure 5.3 (a). Similarly, in Figure 5.3 (b), the input signal,  $I_B$ , varies in the active region and a portion of the negative cycle, reaches the cutoff region. During this section of the cycle, the transistor is driven to cut-off and act as a switch in a closed circuit. This results in the output voltage  $V_{CE}$  and output current  $I_C$  to have a clipped signal on the negative cycle as shown in Figure 5.3 (b). Hence to avoid a distorted signal, it must be ensured that the transistor operates within the active region.



**Fig. 5.3** Transistor Drove to Cut-Off and Saturation during the Amplification

The operating points of the transistors are essential to ensure the desired amplification process. These operating points are determined by drawing a load line on the output characteristics.

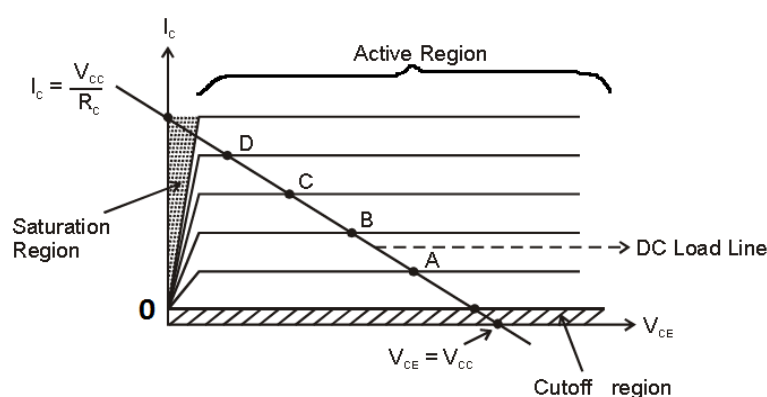
### 5.2.1 Load Lines

The load lines are lines drawn on the output characteristics of the transistor, which helps in determining the operating point for the transistor. In order to adjust the operating point of the transistor within the desired load line, biasing should be proper for the circuit. Load lines are classified as

1. DC load lines
2. AC load lines

#### DC Load Line

DC load line is a line drawn on the output characteristics of the transistor. DC load line has extreme points meeting the  $x$  axis parameter  $V_{CE}$  at  $V_{CC}$  and  $y$  axis parameter  $I_C$  at  $V_{CC}/R_C$ . DC load line is plotted in Figure 5.4. The DC load line meets the output characteristics at various points such as A, B, C and D. These points are the quiescent point or Q point or the operating points.



**Fig. 5.4 DC Load Line**

On the output characteristics, plotted between  $I_C$  vs  $V_{CE}$ , the DC load line is a line having a slope of  $-1/R_C$ . We get the  $x$  intercept when

$$I_C = 0 \Rightarrow V_{CE} = V_{CC}$$

and  $y$  intercept

$$\text{When } V_{CE} = 0 \Rightarrow I_C = V_{CC} / R_C.$$

The line is called a DC load line because on applying the DC conditions, that is removing the AC components such as AC signal source, capacitors and inductors, the intercepts of  $x$  and  $y$  intercepts are obtained.

### AC Load Line

- AC load line is a line intersecting the Q point of the DC load line.
- AC load line is different from the DC load line.
- AC load line is a combination of different slopes plotted between the saturation point and the cutoff points calculated for different operating frequencies of the transistor.
- AC load line is calculated using the AC equivalent circuit parameters that take to account the AC signal source and AC components such as capacitors and inductors. As a limiting case, the capacitors can be short-circuited, assuming the frequency to be infinite.
- At the same time, the DC voltages (the biasing voltage) is short-circuited.
- The AC equivalent circuit to plot the AC load line is given in Figure 5.5 (a) and the AC load line along with the DC load line are given in Figure 5.5 (b).

## NOTES

## NOTES

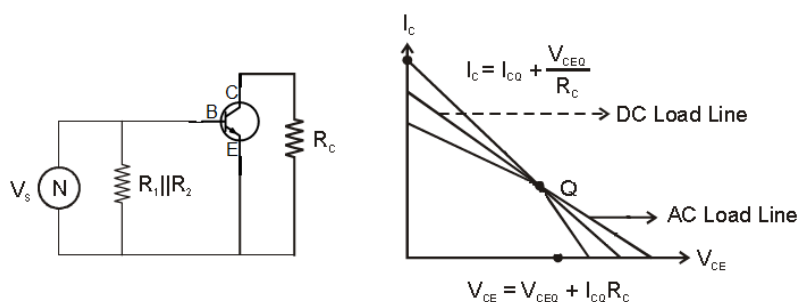


Fig. 5.5 AC Load Line

- AC load line has the limits as

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_C}$$

$$V_{CE} = V_{CEQ} + I_{CQ} R_C$$

- The AC equivalent circuit shows with the DC voltage shorted resulting the resistances  $R_1 \parallel R_2$  and  $R_C$  grounded.

### The Equivalent Circuit of a Transistor Amplifier

Transistors are widely used as amplifiers and it is important to understand the working of transistors as amplifiers through an equivalent circuit approach. Based on the working of the transistor in different frequency ranges, there are two types of analysis of BJTs. They are

- Small signal analysis
- Mid-frequency analysis and
- Low-frequency analysis

The scope of this text covers the small signal analysis of the transistors while operating as amplifiers.

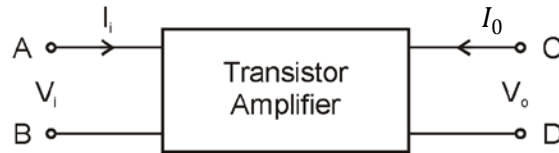
#### 5.2.2 Small Signal Analysis of the Amplifiers

Transistors are nonlinear devices. It is not simple to analyze a nonlinear device. However, on observing the output characteristics, the active region of the transistor is approximately a linear region. Hence input signals of small magnitude can be applied and the circuits can be analyzed through an equivalent circuit model. Such analysis is called as **small signal equivalent circuit analysis**. The small signal analysis will be carried out using two port network theory. There are different parameter models such Z parameter, Y parameter, ABCD parameter, H parameter, G parameter, S parameter etc., H parameter model is a hybrid parameter model which takes into account all the parameters such as input impedance, output impedance, current gain and voltage gain. In small signal equivalent circuit analysis,

the transistor is considered to be a two port network as described in the upcoming section.

### 5.2.3 Hybrid Equivalent Circuits of Two Port Networks

Consider a transistor amplifier represented as a two port network as shown in Figure 5.6.



**Fig. 5.6** Input-Output Ports of a Transistor Amplifier

In Figure 5.6,  $V_i, I_i$  are the input voltage and current respectively at port AB.  $V_o, I_o$  are the output voltage and current respectively at port CD. The H parameter equations are given as

$$\begin{aligned} V_i &= h_{11}I_i + h_{12}V_o \\ I_o &= h_{21}I_i + h_{22}V_o \\ \Rightarrow \begin{bmatrix} V_i \\ I_o \end{bmatrix} &= \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_i \\ V_o \end{bmatrix} \end{aligned}$$

Shorting output terminals CD,  $V_o = 0$ , then

$$h_{11} = \frac{V_i}{I_i} = \text{Input Impedance } (\Omega) = h_i$$

$$h_{21} = \frac{I_o}{I_i} = \text{Forward current gain } (-) = h_f$$

Open circuiting the input terminals AB,  $I_i = 0$ , then

$$h_{12} = \frac{V_i}{V_o} = \text{Reverse voltage Gain } (-) = h_r$$

$$h_{22} = \frac{I_o}{V_o} = \text{Output admittance } (\text{S}) = h_o$$

### Re-Representation of H Parameters with Hybrid Equivalent Circuit

The H parameters will be re-represented to suit the transistor analogy as below.

$$V_i = h_i I_i + h_r V_o$$

$$I_o = h_f I_i + h_o V_o$$

The hybrid equivalent circuit of BJT is given in Figure 5.7.

### NOTES

## NOTES

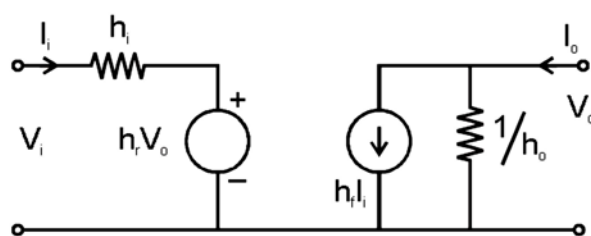


Fig. 5.7 The Hybrid Equivalent Circuit of Transistor

The hybrid equivalent circuit for three different configurations of transistors is given below.

For common emitter configuration, the parameters will have a suffix 'e'.

For common base configuration, the parameters will have a suffix 'b'.

For common collector configuration, the parameters will have a suffix 'c'.

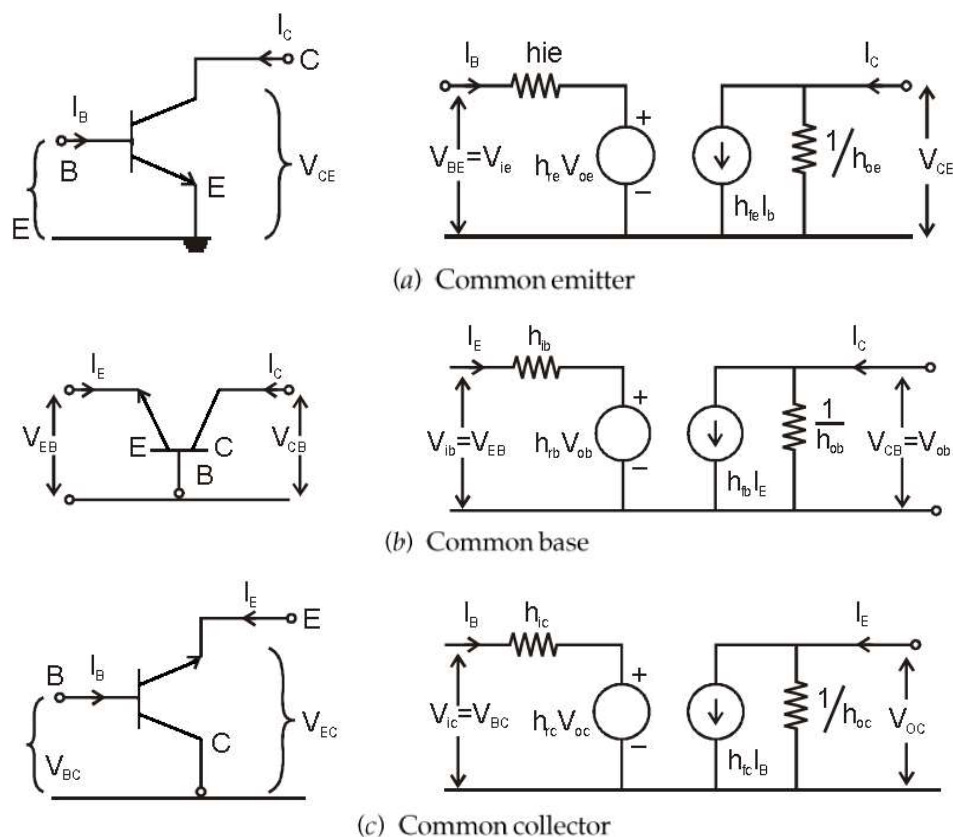


Fig. 5.8 The Hybrid Equivalent Circuit of Different Configurations of a Transistor

### 5.2.4 Small Signal Amplifier Analysis using H Parameters - General Model

Having understood the basic hybrid equivalent model of the BJT, analysis of the BJT for small signal analysis can be explained better with a practically relevant RC

coupled amplifier in this section. However, for the sake of simplicity, a common emitter amplifier will be analyzed and any other configuration can be built upon from the described model by replacing the suffixes of the analyzed parameter.

Following parameters will be analyzed for the common emitter amplifier structure shown in Figure 5.9.

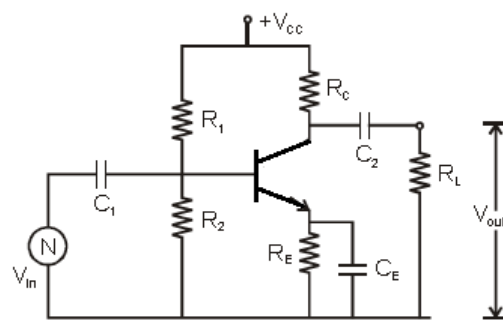
- Current gain
- Voltage gain
- Input impedance
- Output admittance

### Steps for Analysis

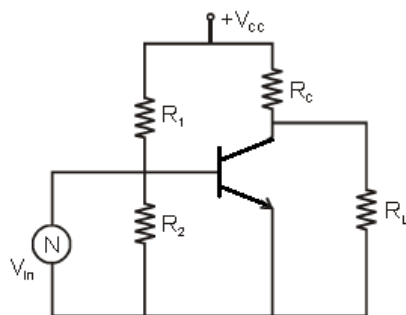
Following steps are to be followed to perform the small signal analysis of the BJT amplifier.

1. For the given amplifier circuit, replace all the capacitors of the circuit with a short circuit.
2. Replace the dc biasing voltage source with a short circuit.
3. Redraw the circuit with terminals connected properly to the ground.
4. Replace the transistor with the hybrid equivalent circuit shown in Figure 5.8.

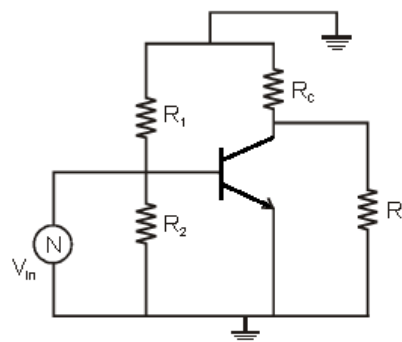
### RC Coupled Amplifier Equivalent Circuit - An Example



(a) RC Coupled amplifier



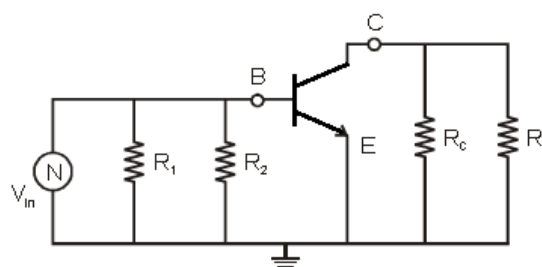
(b) Capacitors short circuited



(c)  $V_{CC}$  - short circuited

### NOTES

## NOTES



(d) Circuit redrawn

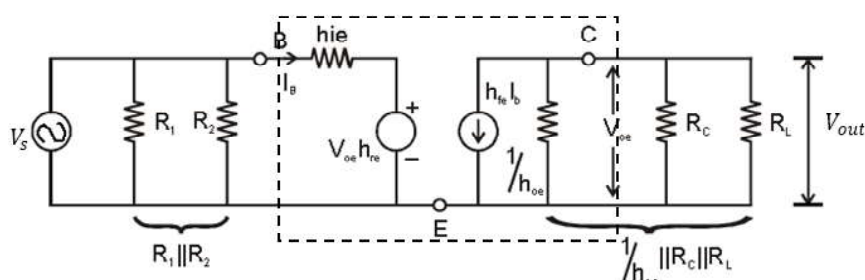


Fig. 5.9 Small Signal Analysis Steps for an RC Coupled Amplifier

## General Model

A general amplifier model is considered for analysis for the circuit shown in Figure 5.10. The analysis is carried out considering that the source voltage consists of an internal source resistance,  $R_s$ . In case the source resistance is to be neglected, then the value of  $R_s$  needs to be equated to zero.

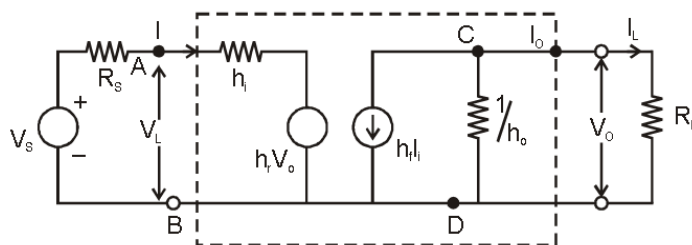


Fig. 5.10 Hybrid Equivalent Circuit for a General Amplifier Circuit

Current gain,  $A_i$ :

$$\text{Input current} = I_i$$

$$\text{Output current} = I_o = -I_L$$

$$\text{Current gain, } A_i = \frac{\text{Output current}}{\text{Input current}} = \frac{+I_L}{I_i} = \frac{-I_o}{I_i} \quad (1)$$

Applying KCL at C,

$$h_f I_i + \frac{V_o}{V_{ho}} = I_o \quad (2)$$

$$I_o = h_f I_i + V_o h_o \quad (3)$$

But  $V_o = I_L R_L = -I_O R_L \quad [\because I_L = -I_O]$

$$\Rightarrow I_O = h_f I_i + (-I_O R_L) h_o$$

$$I_O = h_f I_i - I_O R_L h_o$$

$$I_O + I_O R_L h_o = h_f I_i$$

$$I_O (1 + R_L h_o) = h_f I_i$$

$$A_i = \frac{I_O}{I_i} = \frac{h_f}{1 + h_o R_L} \quad (4)$$

Input impedance,  $Z_i$ :

$$Z_i = \frac{V_i}{I_i} \quad (5)$$

Applying KVL in the input loop,

$$V_s - I_i R_s - I_i h_i - h_r h_o V_o = 0 \quad [\text{Including } V_s] \quad (6a)$$

$$V_i - I_i h_i - h_r V_o = 0 \quad [\text{Only for Amplifier Input}]$$

$$V_i = I_i h_i + h_r V_o \quad (6b)$$

$$\frac{V_i}{I_i} = h_i + h_r \frac{V_o}{I_i} \quad (7)$$

$$V_o = I_L R_L = -I_O R_L$$

$$V_o = +A_i I_i R_L \quad [\text{from 1}] \quad (8)$$

$$\Rightarrow \frac{V_i}{I_i} = h_i + h_r \frac{(A_i I_i R_L)}{I_i}$$

$$Z_i = \frac{V_i}{I_i} = h_i + h_r A_i R_L \quad (9)$$

Substituting equation (4) in equation (9),

$$Z_i = h_i + h_r R_L \left[ \frac{h_f}{1 + h_o R_L} \right] \quad (10)$$

Rearranging for  $R_L$

$$Z_i = h_i + \frac{h_r h_f R_L \times \left( \frac{1}{R_L} \right)}{(1 + h_o R_L) \times \left( \frac{1}{R_L} \right)}$$

$$= h_i + \frac{h_r h_f}{\left( \frac{1}{R_L} + h_o \right)}$$

$$\boxed{Z_i = h_i + \frac{h_f h_r}{h_o + Y_L}} \quad \text{where} \quad Y_L = \frac{1}{R_L} \quad (11)$$

## NOTES



Voltage gain,  $A_v$ :

$$\text{Voltage gain, } A_v = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_o}{V_i} \quad (12)$$

**NOTES**

From equation (8)

$$V_o = A_i I_i R_L$$

Therefore,

$$A_v = \frac{A_i I_i R_L}{V_i} = A_i R_L \left( \frac{I_i}{V_i} \right)$$

$$\boxed{A_v = \frac{A_i R_L}{Z_i}}$$

(13)

Output admittance,  $Y_o$ :

$$\text{Output admittance, } Y_o = \frac{I_o}{V_o}$$

From equation (2),

$$I_o = h_f I_i + V_o h_o$$

$$\frac{I_o}{V_o} = h_f \frac{I_i}{V_o} + h_o \quad (14)$$

From equation 6(a),

$$V_s - I_i R_s - I_i h_i - h_r v_o = 0$$

For  $V_s = 0$ ,

$$I_i R_s + I_i h_i + h_r V_o = 0$$

$$I_i (R_s + h_i) = -h_r V_o$$

$$\frac{I_i}{V_o} = -\frac{h_r}{R_s + h_i} \quad (15)$$

Substituting equation (15) in equation (14),

$$Y_o = \frac{I_o}{V_o} = h_f \left[ \frac{-h_r}{R_s + h_i} \right] + h_o$$

$$\boxed{Y_o = h_o - \frac{h_f h_r}{R_s + h_i}} \quad (16)$$

Summary:

$$A_i = \frac{h_f}{1 + h_o R_L} \quad A_v = \frac{A_i R_L}{Z_i}$$

$$Z_i = h_i + \frac{h_f h_r}{h_o + Y_L}$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

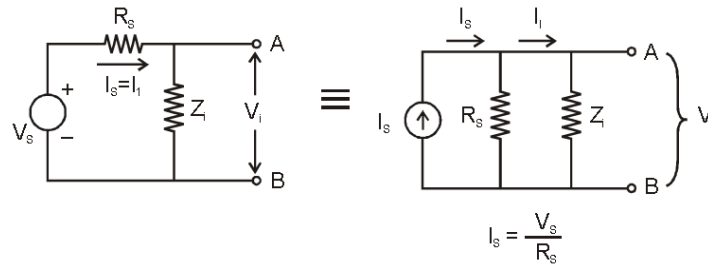
Including the source resistance:

Voltage gain,  $A_{vs}$ :

$$A_{vs} = \frac{\text{Output voltage}}{\text{Input source voltage}} = \frac{V_o}{V_s} \quad (17)$$

$$A_{vs} = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = A_v \frac{V_i}{V_s} \quad (18)$$

Thevenin and Norton's equivalent circuits are as shown in Figure 5.11,



**Fig. 5.11** Thevenin and Norton Equivalent Circuits

$$V_i = V_s \frac{Z_i}{Z_i + R_s} \Rightarrow \frac{V_i}{V_s} = \frac{Z_i}{Z_i + R_s}$$

$$\Rightarrow \boxed{A_{vs} = A_v \cdot \frac{Z_i}{Z_i + R_s}} \quad (19)$$

Current Gain:

$$A_{is} = \frac{I_o}{I_s} = \frac{I_o}{I_i} \times \frac{I_i}{I_s} \quad (20)$$

## NOTES

From Norton equivalent circuit,

$$I_i = I_s \frac{R_s}{R_s + Z_i} \Rightarrow \frac{I_i}{I_s} = \frac{R_s}{R_s + Z_i} \quad (21)$$

## NOTES

$$\Rightarrow \boxed{A_{is} = A_i \frac{R_s}{R_s + Z_i}} \quad (22)$$

Summary:

$$A_{vs} = A_v \cdot \frac{Z_i}{Z_i + R_s} \quad (19)$$

$$A_{is} = A_i \cdot \frac{R_s}{Z_i + R_s} \quad (22)$$

Dividing equation (19) by equation (22)

$$\frac{A_{vs}}{A_{is}} = \frac{A_v \cdot \left( \frac{Z_i}{R_s + Z_i} \right)}{A_i \cdot \left( \frac{R_s}{R_s + Z_i} \right)}$$

Also, substituting for  $A_v$  from equation (13),

$$\Rightarrow \frac{A_{vs}}{A_{is}} = \frac{A_L \frac{R_L}{Z_i}}{A_L} \times \frac{Z_i}{R_s}$$

$$\frac{A_{vs}}{A_{is}} = \frac{R_L}{R_s}$$

$$\boxed{A_{vs} = A_{is} \frac{R_L}{R_s}} \quad (24)$$

Power gains  $A_p$ :

$$A_p = \frac{V_o I_o}{V_i I_i} = \frac{\text{Output power}}{\text{Input power}}$$

$$A_p = A_v \cdot A_i = \left[ A_i \frac{R_L}{Z_i} \right] A_i$$

$$\boxed{A_p = A_i^2 \frac{R_L}{Z_i}}$$

## Gain Bandwidth Product

The gain-bandwidth product of a CE amplifier is given as

$$G - BW = A_v \times (BW)$$

$$= A_v \times (f_2 - f_1)$$

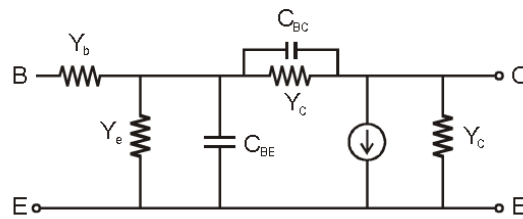
Where  $f_2$  and  $f_1$  are lower cut off frequency and higher cut off frequency.

Transistor Amplifier

$$GBW = -\frac{h_{fe}R_L}{h_{ie} + R_s} \times \frac{1}{2\pi R_{eq}C_{eq}}$$

### High-Frequency Analysis of an Amplifier

The hybrid circuit model discussed so far are suitable for low-frequency analysis. Recalling that in making a small signal analysis, the capacitances in the circuit were neglected or short-circuited. For high-frequency analysis, the internal capacitances of the transistors across various junctions, and the output coupling capacitors must be included for analysis. The hybrid model discussed does not provide a stable satisfactory analysis. Hence the hybrid  $\pi$  model as shown in Figure 5.12 must be included.



**Fig. 5.12** The Equivalent Circuit for High-Frequency Analysis of BJT

Where

- $C_{BE}$  = Forward biased base emitter junction capacitance.
- $C_{BC}$  = Reverse biased base collector junction capacitance.
- $V_b, V_c, R_c$  = Internal junction resistances.

### Check Your Progress

1. What is the significance of load lines?
2. What are the two types of load lines?

## 5.3 POWER AMPLIFIERS

Semiconductor devices like transistors handles the small magnitude of power of the order of few mW's are of no practical use. Hence the need for large amplifiers with the ability to handle large power without the loss of gain is important to be discussed and analyzed. The output of the power amplifiers is directly fed to the high power loads like audio systems, loudspeakers, DC motor control drives etc.

Power amplifiers have a greater swing of voltages while operating in the active regions. Based on the input and output voltage swing of the amplifiers they are classified as below:

- (i) Class A amplifier
- (ii) Class B amplifier

### NOTES

## Output Characteristics of An Amplifier

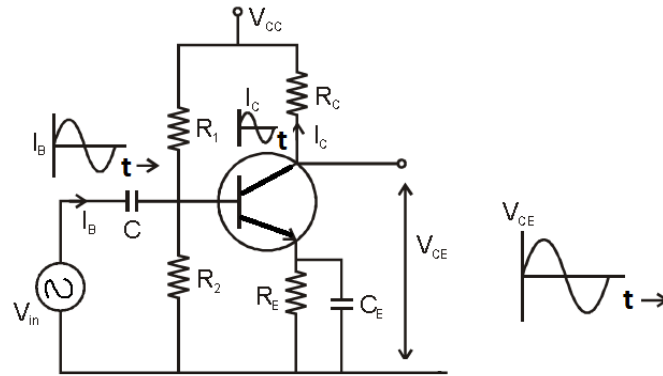
For proper amplification to take place, the transistor must operate in the active region. Operating in the active or in the saturation region results in transistor operating as a switch.

Those amplifiers, in which the transistor operates only in the active region as shown in Figure 5.13 are called as class *A amplifiers*. Class A amplifiers provide a complete  $360^\circ$  cycle of output signals (both voltage and current) for a  $360^\circ$  cycle of input signals.

94 *Self-Instructional  
Material*

$A_i$  and  $C_i$  gets converted to the output current points  $Q_{iv}$ ,  $A_{iv}$  and  $C_{iv}$ . The conversion input signal to the output signals as depicted by dashed lines in Figure 5.13 never cross the saturation or cut off region. Input signal  $Q_i$  gets amplified to  $Q_{ov}$  and  $Q_{or}$ ,  $A_i$  gets amplified to  $A_{ov}$  and  $A_{or}$ , and,  $C_i$  gets amplified to  $C_{ov}$  and  $C_{or}$ . Since the input signal is sinusoidal, the output signals are also sinusoidal without any distortions.

A simple class A amplifier circuit is shown in Figure 5.14. The various signals such as input voltage, the input current  $I_B$ , output voltage  $V_{CE}$ , and output current  $I_C$  are shown in the Figure 5.14.



**Fig. 5.14** Class A Amplifier

The efficiency of class A amplifiers is approximately 25%. This is because they operate over a complete  $360^\circ$  cycle resulting in a huge power loss. The general expression for efficiency for a class A amplifier is given as:

$$\eta\% = \left\{ \frac{[V_{ce(max)} - V_{ce(min)}][I_{c(max)} - I_{c(min)}]}{8V_{CC}I_{CQ}} \right\} \times 100$$

### Efficiency Calculation of Class A Amplifier

Let the efficiency be  $\eta$

$$\eta = \frac{\text{output power}}{\text{input power}}$$

Output power is an AC output power and input power is a combination of both ac and dc input power. DC input power is due to the biasing input provided to the amplifier. AC input power is due to the small signal input power provided. Generally, DC input power is much larger than the AC input power.

Therefore,

$$\eta = \frac{P_o(ac)}{P_{in}(dc) + P_{in}(ac)} \approx \frac{P_o(ac)}{P_{in}(dc)}$$

## NOTES

We know that,

$$P_{in}(ac) = V_Q I_Q = \frac{V_{CC}}{2} \frac{V_{CC}}{2R_L}$$

## NOTES

The RMS ac output power,

$$P_o(ac) = \frac{V_{CC}}{2\sqrt{2}} \times \frac{V_{CC}}{2\sqrt{2}R_L}$$

$$P_o(ac) = \frac{V_{CC}^2}{8R_L}$$

$$P_{in}(dc) = V_{CC} \times I_C = V_{CC} \times \frac{V_{CC}}{2R_L}$$

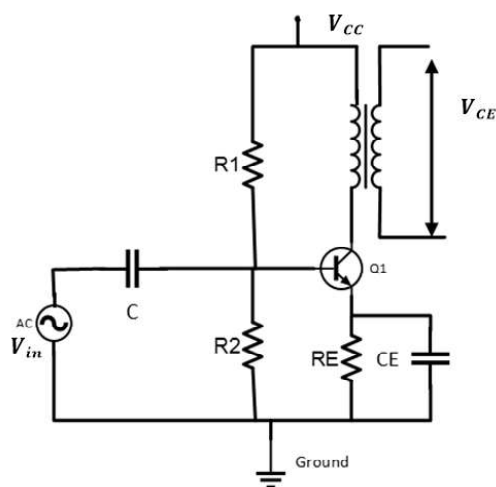
$$P_{in}(dc) = \frac{V_{CC}^2}{2R_L}$$

Therefore,

$$\eta = \frac{P_o(ac)}{P_{in}(dc)} = \frac{\frac{V_{CC}^2}{8R_L}}{\frac{V_{CC}^2}{2R_L}}$$

$$\eta = 25\%$$

Efficiency can be slightly improved by employing transformer coupled class A power amplifier. The circuit diagram of a transformer coupled power amplifier is shown in Figure 5.15.



**Fig. 5.15** Transformer Coupled Class A Transformer

The efficiency of a transformer coupled power amplifier is approximately 50%. The general expression for efficiency is given as

$$\eta\% = 50 \times \left\{ \frac{V_{ce(max)} - V_{ce(min)}}{V_{ce(max)} + V_{ce(min)}} \right\} \times 100$$

Efficiency calculation of a transformer coupled class A amplifier:

$$\eta = \frac{P_o(ac)}{P_{in}(dc)}$$

$$P_o(ac) = \frac{V_o}{\sqrt{2}} \frac{I_o}{\sqrt{2}}$$

We know that,  $V_o = V_{CC}$  and  $I_o = \frac{V_{CC}}{R_L}$ .

$$P_o(ac) = \frac{V_{CC}}{\sqrt{2}} \frac{V_{CC}}{\sqrt{2}R_L} = \frac{V_{CC}^2}{2R_L}$$

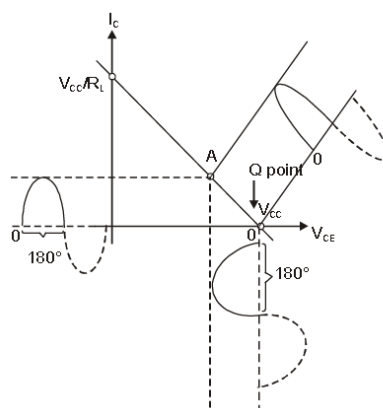
$$P_{in}(dc) = V_{CC} \times I_C = V_{CC} \times \frac{V_{CC}}{R_L}$$

$$P_{in}(dc) = \frac{V_{CC}^2}{R_L}$$

$$\eta = \frac{\frac{V_{CC}^2}{2R_L}}{\frac{V_{CC}^2}{R_L}} = 50\%$$

### 5.3.2 Class B Amplifier

Amplifiers, which produces an output signal only for 180° of the input cycle are said to be class B amplifiers. Half of the input cycle of the signal constitute 180° cycle and the output signal conduction is possible when the selected Q point is such that they lie in the saturation point or cut off point as shown in Figure 5.16.



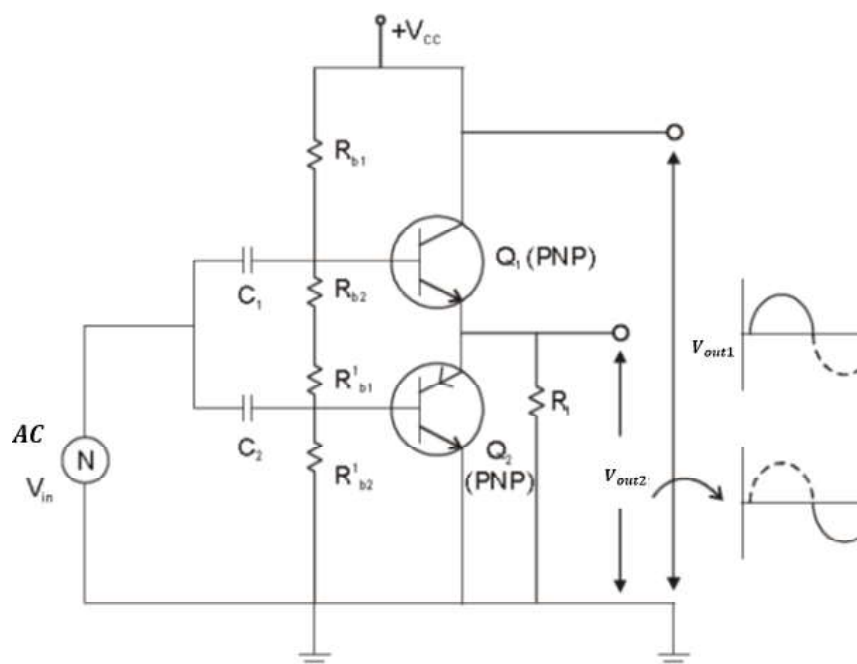
**Fig. 5.16** Input-Output Characteristics of Class B Amplifier

## NOTES



## NOTES

Class B amplifiers are efficient when compared to class A amplifiers as they conduct for only half the cycle and the power loss is prevented in the other half cycle of the amplifier. Since class B amplifiers operate for only one-half of the transistors, a circuit arrangement known as complimentary amplifiers as shown in Figure 5.17 is used. In this circuit setup, out of two transistors, one is PNP and other is NPN transistors are used such that each transistor conducts in one-half cycle of the input cycle.



**Fig. 5.17** Class B Amplifier

The complementary amplifier circuits consists of a PNP-NPN transistors coupled together and are also called as emitter follower circuit. The input signal to these amplifiers is generally fed with an anti-phase signal input. This makes Q1 conduct in the positive half cycle and Q2 conduct in the negative half cycle. The resistance  $R_{b1}$ ,  $R_{b2}$ ,  $R'_{b1}$ ,  $R'_{b2}$  are potential divider bias resistances.

The output terminal is tapped between the PNP and NPN transistor, that is at the emitter terminals of both the transistor. The output signals are generated for one half of the cycle as shown in Figure 5.17. The efficiency of class B push-pull amplifiers is generally 78.5%.

The other type of class B amplifiers is push-pull amplifiers. They employ either both PNP or NPN transistors. Push-pull amplifiers employ center-tapped transformers at both the input and at the output side resulting in a bulkier costly circuit.

Efficiency calculation of class B amplifier:

Efficiency,  $\eta$  is given as

$$\eta = \frac{P_o(ac)}{P_{in}(dc)}$$

$$P_o(ac) = V_o I_o = \frac{1}{2} \frac{V_{cc}}{\sqrt{2}} \frac{I_c}{\sqrt{2}}$$

$$P_o(ac) = \frac{V_{cc} I_c}{4}$$

$$P_{in}(dc) = V_{cc} I_{av} = V_{cc} \frac{I_m}{\pi} = V_{cc} \frac{I_c}{\pi}$$

Therefore,

$$\eta = \frac{P_o(ac)}{P_{in}(dc)} = \frac{\frac{V_{cc} I_c}{4}}{V_{cc} \frac{I_c}{\pi}} = \frac{\pi}{4}$$

$$\eta = 78.5\%$$

## NOTES

### 5.3.3 Class AB Amplifier

Class AB amplifiers are a combination of class A amplifiers and class B amplifiers. The conduction cycle of class AB amplifiers range is greater than  $180^\circ$  and less than  $360^\circ$ . Such type of conduction cycle can be achieved by selecting the Q point slightly higher than the cutoff point on the dc load line of the output characteristics of the transistor. The circuit diagram of class AB amplifier is shown in Figure 5.18. The circuit is similar to the complimentary class B amplifier, except that the base resistances  $R_{b_2}$  and  $R'_{b_1}$  are replaced with diodes  $D_1$  and  $D_2$ . Diodes  $D_1$  and  $D_2$  are connected antiphase with each other. These diodes help in maintaining a forward potential between the emitter potentials of the two transistors thereby shifting the Q point slightly towards the active region from the cut-off region.

## NOTES

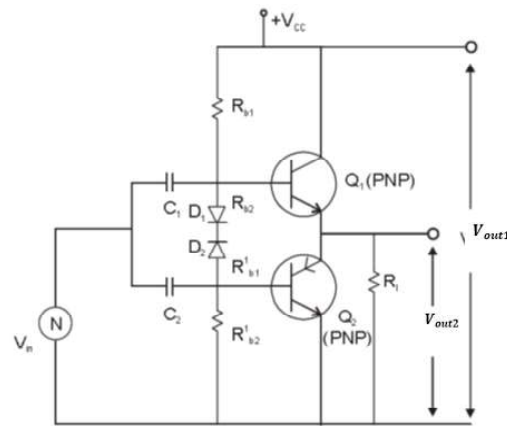


Fig. 5.18 Class AB Amplifier

The output characteristics for class AB amplifiers are shown in Figure 5.19. It is observed from the characteristics that for a control input voltage as shown in Figure 5.19 with a negative clipped current, the output voltage and the output current is also clipped in the negative cycle thereby reducing the conduction cycle from  $360^\circ$ , but higher than  $180^\circ$ .

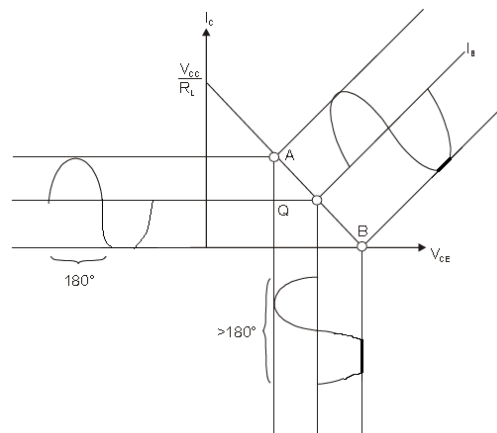
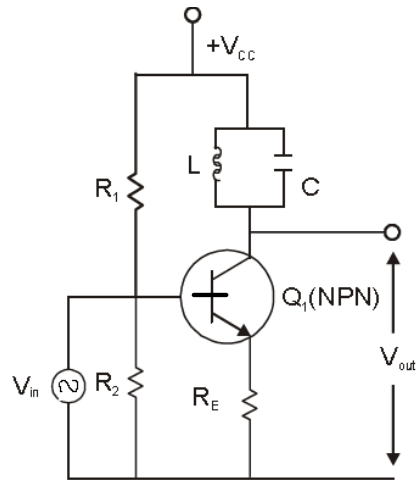


Fig. 5.19 Input-Output Characteristics of Class AB Amplifier

### 5.3.4 Class C Amplifier

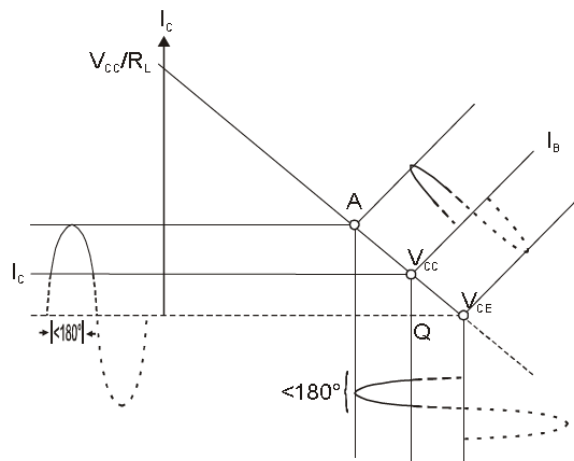
Class C amplifiers are designed for better efficiency greater than class B and AB amplifiers. This is achieved by reducing the conduction cycle less than  $180^\circ$ . Selecting the Q point beyond cutoff in the negative  $I_C$  region results in a conduction cycle less than  $180^\circ$ . Class C amplifiers are generally tuned amplifiers used in wireless communications where the output amplification signal is tuned by a tank circuit. The tank circuit consists of inductor and capacitor connected in parallel to each other in the output circuit. The tank circuit ensures a constant potential between

the LC circuit. The output voltage is the difference between the applied bias voltage  $V_{CC}$  and the tank circuit voltage. Resistors  $R_1$  and  $R_2$  forms the potential divider biasing for the circuit. A simple class C amplifier is shown in Figure 5.20.



**Fig. 5.20** Class C Amplifiers

The output characteristics are as shown in Figure 5.21. As observed from the characteristics the control parameter base current conducts for less than half cycle, i.e.,  $< 180^\circ$ . Therefore, the output voltage,  $V_{CE}$  and the output current,  $I_C$  also conducts for less than half cycle, i.e.,  $< 180^\circ$ . The potential divider resistance are chosen such that the Q points are closer towards the cutoff regions of the output characteristics. Across the tank circuit, the change in voltage or change in current responds to a differential change in their respective values and hence provides a pulse output on fine tuning the values of L and C. their operational linearity when compared to class A and B amplifiers are very poor. such circuits generate large pulses for a short period of time and also have less average power in the circuit. The efficiency of class C amplifier circuits are more than 85%.



**Fig. 5.21** Input-Output Characteristics of Class C Amplifier

## NOTES

## NOTES

## Comparison of Power Amplifiers

Amplifier	Operational linearity	Efficiency
Class A	Extremely linear	25%
Class B	Linear in half the cycle	50% - 75%
Class AB	Linear in less than half cycle	80%
Class C	Very poor	90%

## Characteristics of Power Amplifier

Power amplifiers as described above must have the following basic characteristics.

- Power amplifiers must be able to handle a large magnitude of power.
- Power amplifiers have a large load current.
- Power output is large
- Current gain is low
- High input resistance and
- Low output impedance.

## Crossover Distortion

As the name suggests, the distortion of the output signal at the point of crossing over from positive to negative or negative to positive cycles is called crossover distortion. The main reason for crossover distortion is due to the cut-in voltages ( $V_i$ ) of the transistors. When the transistor approaches to operate in lower voltages less than cut in voltages, they move to the cut-off mode or transistor switches OFF. Only when the signal voltage go beyond the cut-in voltage transistors operate normally in the ON or amplifier mode. Due to distortion, the output wave form as shown in Figure 5.22 occurs.

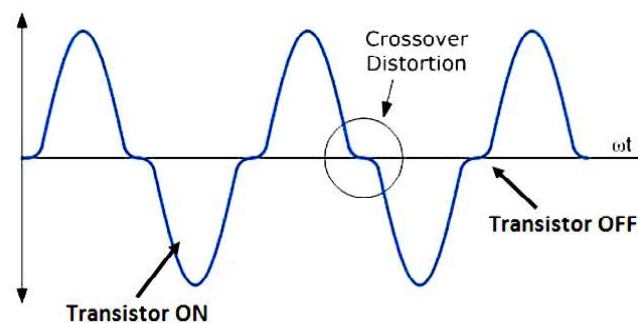


Fig. 5.22 Crossover Distortions in Power Amplifiers

In order to eliminate crossover distortions, push-pull amplifiers, the bypass diodes, complementary symmetry structures of PNP-NPN transistors are used. Push-pull amplifiers employ two types of transistors PNP and NPN to push and

pull the output voltage from  $+V_{CC}$  and Ground. A simple class A push pull amplifier is shown in Figure 5.23. The class A push pull amplifier employs two centre tapped transformers. The input voltage from the primary side of the transformer is split into two signals that are anti-phase with each other on the secondary side of the transformer. The resistors  $R_1$  and  $R_2$  form the potential divider for the DC bias voltage. The transistor  $Q_1$  amplifies the input signal in one half and the transistor  $Q_2$  amplifies the signal in the other half of the input cycle. The centre tapped amplified voltage is tapped across the secondary side of the transformer as shown in figure 2.31.

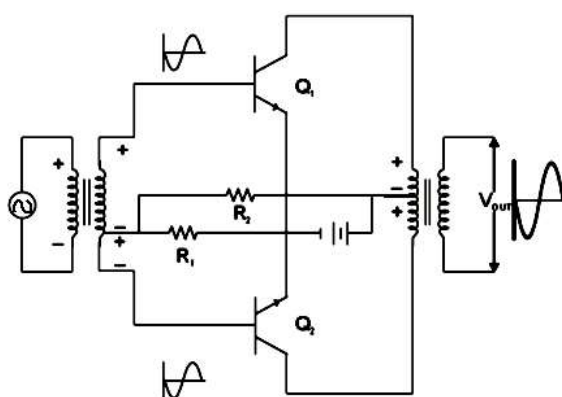


Fig. 5.23 Class A Push-Pull Amplifier

### Important Formula

- DC load line: when  $I_C = 0 \Rightarrow V_{CE} = V_{CC}$   
when  $V_{CE} = 0 \Rightarrow I_C = V_{CC} / R_C$

- AC load line:

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_C}$$

$$V_{CE} = V_{CEQ} + I_{CQ} R_C$$

- H parameter equations:

$$V_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$

$$h_{11} = \frac{V_i}{I_i} = \text{Input Impedance } (\Omega) = h_i$$

$$h_{21} = \frac{I_o}{I_i} = \text{Forward current gain } (-) = h_f$$

$$h_{12} = \frac{V_i}{V_o} = \text{Reverse voltage Gain } (--) = h_r$$

### NOTES

$$h_{22} = \frac{I_o}{V_o} = \text{Output admittance (}\mathfrak{Y}\text{)} = h_o$$

**NOTES****Check Your Progress**

3. What are the different types of power amplifier?
4. What is crossover distortion?

## 5.4 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

1. The load lines are lines drawn on the output characteristics of the transistor, which helps in determining the operating point for the transistor.
2. DC and AC are the two types of load lines.
3. Class A, Class B, Class AB and Class C are the types of power amplifier.
4. The distortion of the output signal at the point of crossing over from positive to negative or negative to positive cycles is called crossover distortion.

## 5.5 SUMMARY

- Transistors may be used as amplifiers, switch in ON position and switch in OFF position.
- When transistors operate in the region specified below, their applications vary
  - o In active region - acts as amplifier
  - o In saturation region - acts as a switch in ON mode
  - o In cut-off region - acts as switch in OFF mode
- Load lines are lines drawn on the output characteristics of the transistors.
- Point of intersection of the DC load line and the output characteristics are called as Q point or quiescent point.
- The small signal analysis may be done using the hybrid parameters.
- H parameters relation is given as

$$V_i = h_{11} I_i + h_{12} V_o$$

$$I_o = h_{21} I_i + h_{22} V_o$$

- $h_{11}$  represents the input impedance,  $h_{21}$  represents the forward current gain,  $h_{12}$  represents the reverse voltage gain and  $h_{22}$  represents the output admittance.
- Emitter follower circuits are generally used as impedance matching circuit.

## 5.6 KEY WORDS

- **Power amplifier:** It is an amplifier used to increase the magnitude of power of a given input signal.
- **Efficiency of an amplifier:** It represents the amount of AC power delivered (transferred) from the DC source.
- **Crossover distortion:** It is the term given to a type of distortion that occurs in push-pull class AB or class B amplifiers. It happens during the time that one side of the output stage shuts off, and the other turns on.

## NOTES

## 5.7 SELF ASSESSMENT QUESTIONS AND EXERCISES

### Short Answer Questions

1. What are the different types of power amplifier?
2. What do you mean by crossover distortion?
3. What is the difference between the small signal and large signal analysis?
4. What do you mean by DC load line?
5. Mention the importance of the DC load line?
6. What are hybrid parameters?
7. What are the different modes of operation of the transistor?
8. Draw the equivalent circuit of the transistor in different modes of operation.
9. Mention the difference between the DC load line and AC load line
10. Draw the equivalent circuit of the RC coupled amplifier.
11. Define gain-bandwidth product.
12. Compare the efficiencies of different power amplifiers.
13. Compare the linearity's of different power amplifiers.
14. Mention the methods to avoid crossover distortion.
15. Draw the diagram of the class A push-pull amplifier.
16. Draw the output characteristics of a class A amplifier.
17. Mention the expression for a current gain of the different transistor derived using h parameters.

### Long Answer Questions

1. Derive the expression for current gain for a common emitter transistor using h parameters.



## NOTES

2. Explain the working principle of class A amplifiers with neat diagram and output characteristics. Also, derive the efficiency for the class A amplifier.
3. Explain the working principle of class B amplifiers with neat diagram and output characteristics. Also, derive the efficiency for the class B amplifier.
4. Explain the working principle of class AB amplifiers with neat diagram and output characteristics. Also, derive the efficiency for the class AB amplifier.

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## 5.8 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

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## UNIT 6 TRANSISTOR BIASING

### Structure

- 6.0 Introduction
- 6.1 Objectives
- 6.2 Transistor Biasing
  - 6.2.1 Stability Factors
  - 6.2.2 Biasing Methods
  - 6.2.3 Fixed Bias Method or Base Resistor Method
  - 6.2.4 Collector Base Bias Method
  - 6.2.5 Self-Bias or Potential/Voltage Divider Bias
- 6.3 Answers to Check Your Progress Questions
- 6.4 Summary
- 6.5 Key Words
- 6.6 Self Assessment Questions and Exercises
- 6.7 Further Readings

### NOTES

## 6.0 INTRODUCTION

In this unit, you will learn about the transistor biasing. It is process of applying DC operating current or voltage conditions to the optimum level so that applied AC input signal can be amplified correctly. The biasing of the transistors may be categorized based on the forward and reverse biasing of the two junctions of the transistors. Additionally, based on the application of the transistors and the stability of the transistors, the biasing techniques are classified based on the type of feedback network. In this chapter, different techniques of transistor biasing techniques and stability analysis of each type of biasing technique will be discussed.

## 6.1 OBJECTIVES

After going through this unit, you will be able to:

- Define the term transistor biasing
- Discuss the stability factors
- Explain the various methods of transistor biasing

## 6.2 TRANSISTOR BIASING

Biasing is a process of making the transistor operate satisfactorily as an amplifier by providing external DC bias voltage and circuitry.

- Transistor operates as an amplifier when working in the active region
- Transistor operates as a switch, when working in the cut-off region and saturation region.

**NOTES**

- The operating point tends to shift or oscillate between different regions due to the variation of the collector current  $I_C$  and  $\beta$ . Hence holding the operating point within the active region throughout the duration of operation is a complex task manually.

- Hence a biasing circuitry coupled with a dc bias voltage makes the instability of the operating point, stable.

The operating point or the Q point is dependent on the following parameters

- (i) The collector current
- (ii) The base current
- (iii) Input applied signal voltage
- (iv) The  $\beta$  factor of the diode

The above parameters are to be kept within a stable region to make the transistor operate in the active region.

**6.2.1 Stability Factors**

It is important to understand the stability factor governing the transistor biasing. Stability factors depend on the collector current,  $I_C$ , collector current due to minority carriers,  $I_{C0}$ , the current gain parameter,  $\beta$  and the base-emitter voltage  $V_{BE}$ . The stability factor are of three types based on the controlling parameters.

$$(i) \quad S = \frac{\partial I_C}{\partial I_{C0}} \quad \text{at constant } V_{BE}, \beta.$$

$$(ii) \quad S' = \frac{\partial I_C}{\partial V_{BE}} \quad \text{at constant } I_{C0}, \beta.$$

$$(iii) \quad S'' = \frac{\partial I_C}{\partial \beta} \quad \text{at constant } I_{C0}, V_{BE}.$$

The general expression for the stability factor  $S$  in a common emitter configuration is given as

$$S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

**Proof:**

The collector current in a CE configuration is given as

$$I_C = I_{majority} + I_{minority}$$

$$I_C = I_C(\text{majority}) + I_{CEO}$$

$$I_C = \beta I_B + I_{CEO} \quad \therefore I_C = \beta I_B$$

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

Partially differentiating the above expression,

$$\partial I_C = \beta \partial I_B + (1 + \beta) \partial I_{CBO}$$

$$1 = \frac{\beta \partial I_B}{\partial I_C} + \frac{(1 + \beta) \partial I_{CBO}}{\partial I_C}$$

$$\frac{(1 + \beta) \partial I_{CBO}}{\partial I_C} = 1 - \frac{\beta \partial I_B}{\partial I_C}$$

$$\frac{\partial I_{CBO}}{\partial I_C} = \frac{\left(1 - \frac{\beta \partial I_B}{\partial I_C}\right)}{(1 + \beta)}$$

We know that stability factor,  $S = \frac{\partial I_C}{\partial I_{CBO}}$ ,

Therefore,

$$S = \frac{(1 + \beta)}{\left(1 - \frac{\beta \partial I_B}{\partial I_C}\right)}$$

Using the above general expression, for each biasing technique the differential ratio  $\frac{\partial I_B}{\partial I_C}$  will be determined by using KVL and current relations for the transistor.

### 6.2.2 Biasing Methods

The transistor can be biased by the following methods.

- (i) Fixed bias method or base resistor method
- (ii) Collector base bias method
- (iii) Self-bias or potential divider bias

In the following section, we'll examine each biasing method and determine the stability factor. It is to be noted that in all the biasing methods, the following steps are to be followed.

#### Steps to Analyze the Biasing Circuit

- Apply KVL in the input loop of the biasing circuit.

## NOTES

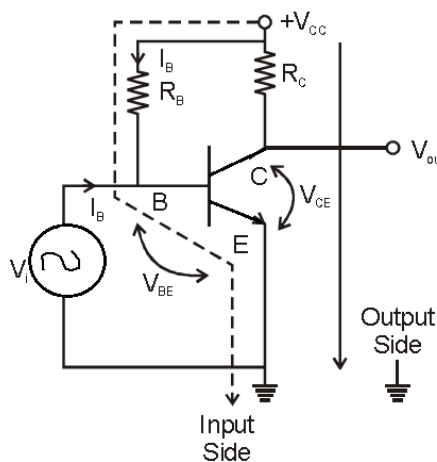
**NOTES**

- Rearrange the expression to obtain the expression in terms of  $I_B$ .
- Apply KVL in the output loop and obtain the expression for  $I_C$  or  $V_{CE}$ .
- Substitute in the stability factor expression  $S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$  to determine the stability of the biasing method.
- The stability factor must be as less as possible and must be independent of the temperature affecting parameters such as  $\beta$ ,  $I_{C0}$  and  $I_C$ .

**6.2.3 Fixed Bias Method or Base Resistor Method**

The circuit diagram for the fixed bias method is shown in Figure 6.1. The circuit as the name implies has a fixed base resistor connected between the base terminal and the supply voltage  $V_{CC}$ . The base resistor,  $R_B$  is connected between the DC bias  $V_{CC}$  and the base terminal of the NPN transistor. For the purpose of analysis, KVL is applied on the input side (shown in the dotted line in Figure 6.1) and the output side (shown as a dotted line in Figure 6.1). Input AC voltage is applied between the terminal base and emitter. Emitter terminal is shorted to ground potential. The collector terminal is connected to the output collector resistance. The base emitter voltage exhibits a forward diode breakdown potential of 0.7 volts for silicon based transistors. The relation between the base current and collector terminal for a common emitter configuration is recalled as below:

$$\beta = \frac{I_C}{I_B}$$



**Fig. 6.1** Fixed Bias Method or Base Resistor Method

All the biasing method analysis is DC analysis and hence the AC related components are open circuited. It is to be recalled that for DC voltage  $X_C = \infty$  (open circuited).

Applying KVL on the input side, from  $V_{CC}$  to ground through  $V_{BE}$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad (1)$$

Applying KVL on the output side, from  $V_{CC}$  to ground through  $V_{CE}$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

It is important to know the relation between  $I_C$  and  $I_B$

$$I_C = \beta I_B$$

**Stability factor, S:**

$$S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

Differentiating the expression  $I_B$  in (1) with respect to  $I_C$

$$\frac{\partial I_B}{\partial I_C} = 0$$

Therefore,

$$S = (1 + \beta)$$

Normally, the  $\beta$  value of transistors are high ranging from 50 to 200. Hence, the stability factor is also high. Also,  $\beta$  is dependent on  $I_{CO}$  which in turn is dependent on temperature. As the temperature increases in the circuit due to the prolonged operation, the stability factor also changes resulting in an unstable circuit. This makes the Q point move beyond the active region.

## NOTES

**NOTES**

Stability factor  $S'$  :

Stability factor  $S'$  is given as

$$S' = \frac{\partial I_C}{\partial V_{BE}}$$

We know that

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

Also,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Therefore,

$$I_C = \beta \left( \frac{V_{CC} - V_{BE}}{R_B} \right) + (1 + \beta) I_{CBO}$$

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B}$$

Stability factor  $S''$  :

Stability factor  $S''$  is given as

$$S'' = \frac{\partial I_C}{\partial \beta}$$

We know that

$$I_C = \beta I_B + (1 + \beta) I_{CBO}$$

Also,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Therefore,

$$I_C = \beta \left( \frac{V_{CC} - V_{BE}}{R_B} \right) + (1 + \beta) I_{CBO}$$

$$\frac{\partial I_C}{\partial \beta} = \left( \frac{V_{CC} - V_{BE}}{R_B} \right) + I_{CBO} = I_B + I_{CBO}$$

Neglecting the minority carrier contribution,  $I_{CBO}$

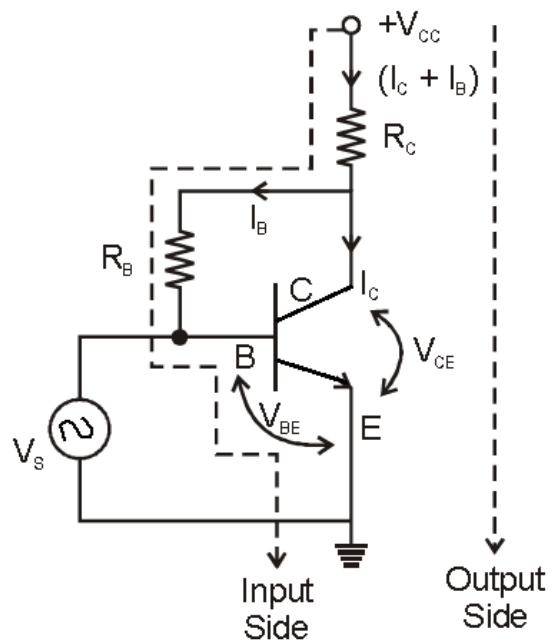
$$\frac{\partial I_C}{\partial \beta} \approx I_B \approx \frac{I_C}{\beta}$$

Summarising all the stability factors for a fixed bias method,

$$S = \frac{\partial I_C}{\partial I_{CO}} = (1 + \beta) \quad S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B} \quad S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}$$

#### 6.2.4 Collector Base Bias Method

The collector to base bias circuit is shown in Figure 6.2. The difference between the fixed bias circuit and the collector base bias circuit is that the base resistor is connected to the collector terminal rather than to the supply voltage terminal. This slight change improves the stability factor considerably. Now, the current across the collector resistance  $R_C$  will be the sum of the base current and the collector current  $I_B + I_C$ . Since the collector current is now increased by a fraction equivalent to the base current, there is a significant increase in the stability factor,  $\beta$  as shown in the stability analysis section described below.



**Fig. 6.2** Collector Base Bias Method

#### NOTES



The current through the base resistor is  $I_B$ , the current through the resistance  $R_C$  is  $I_C + I_B$ .

**NOTES**

Follow the steps given below for analysis:

Applying KVL on the input side, from  $V_{CC}$  to ground through  $V_{BE}$

$$V_{CC} - (I_B + I_C)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B R_C - I_C R_C - I_B R_B - V_{BE} = 0 \quad (2)$$

$$V_{CC} - I_B R_C - \beta I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (R_C + \beta R_C + R_B)I_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_C} \quad (3)$$

Applying KVL on the output side, from  $V_{CC}$  to ground through  $V_{CE}$

$$V_{CC} - (I_B + I_C)R_C - V_{CE} = 0 \quad V_{CE} = V_{CC} - (I_B + I_C)R_C$$

**Stability factor, S:**

$$S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

Rearranging (2)

$$V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

Differentiating the above expression

$$0 = \partial I_B (R_C + R_B) + \partial I_C R_C + 0 \quad \frac{\partial I_B}{\partial I_C} = - \frac{R_C}{(R_C + R_B)}$$

$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_C}{(R_C + R_B)} \right)}$$

Stability of this type of bias depends largely on the denominator  $\beta$  which is further controlled by the resistances  $R_B$  and  $R_C$ .

Stability factor  $S' = \frac{\partial I_C}{\partial V_{BE}}$  :

We know that

$$V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

$$I_B (R_C + R_B) + I_C R_C = V_{CC} - V_{BE}$$

$$\frac{I_C}{\beta} (R_C + R_B) + I_C R_C = V_{CC} - V_{BE}$$

$$I_C \left\{ \frac{(R_C + R_B) + \beta R_C}{\beta} \right\} = V_{CC} - V_{BE}$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{(R_C + R_B) + \beta R_C}$$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1 + \beta) R_C}$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} = - \frac{\beta}{R_B + (1 + \beta) R_C}$$

Stability factor  $S'' = \frac{\partial I_C}{\partial \beta}$  :

We know that

$$V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

Also, simplifying the above expression for  $I_C$

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1 + \beta) R_C}$$

Using  $\frac{d}{dt} \left( \frac{u}{v} \right) = \frac{\left( v \frac{du}{dt} - u \frac{dv}{dt} \right)}{v^2}$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{\{ (V_{CC} - V_{BE}) [(1 + \beta) R_C + R_B] \} - \{ \beta R_C (V_{CC} - V_{BE}) \}}{[ (1 + \beta) R_C + R_B ]^2}$$

## NOTES

**NOTES**

$$= \frac{(V_{CC} - V_{BE})\{R_C + \beta R_C + R_B - \beta R_C\}}{[(1 + \beta)R_C + R_B]^2}$$

$$= \frac{(V_{CC} - V_{BE})\{R_C + R_B\}}{[(1 + \beta)R_C + R_B]^2}$$

Using the  $I_C$  expression from above,

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C \{R_C + R_B\}}{[(1 + \beta)R_C + R_B]}$$

Summarising the stability factors,

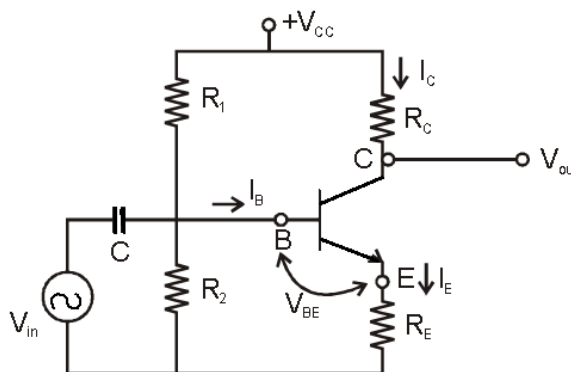
$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_C}{(R_C + R_B)} \right)}$$

$$S' = -\frac{\beta}{R_B + (1 + \beta)R_C}$$

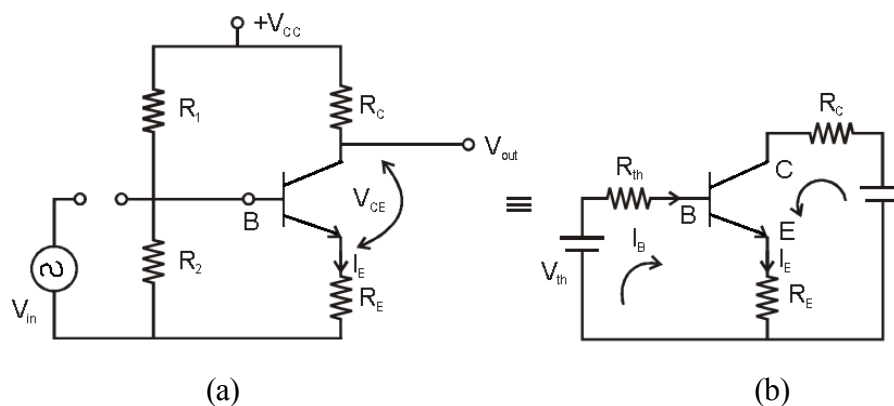
$$S'' = \frac{I_C \{R_C + R_B\}}{[(1 + \beta)R_C + R_B]}$$

**6.2.5 Self-Bias or Potential/Voltage Divider Bias**

The potential divider circuit or the self-bias circuit is shown in Figure 6.3. The resistances  $R_1$  and  $R_2$  act as potential divider circuits for the input DC bias voltage. For the analysis of the potential divider bias circuit, the circuit is redrawn with the dc equivalent circuit model in Figure 6.4 (a). When the capacitor of the actual circuit in Figure 6.3 is redrawn for DC analysis, the input ac voltage source does not have any impact and hence discarded for further analysis. Since the capacitor is an open circuit for dc analysis, the input ac voltage also do not impact the working of the circuit.



**Fig. 6.3** Potential Divider Bias Method or Self-Bias Method



**Fig. 6.4** Equivalent Circuit of Self-Bias Circuit

Further to simplify the analysis, the circuit in Figure 6.4 (a) is redrawn and a Thevenin equivalent circuit is made looking at the bias voltage source,  $V_{CC}$ , potential divider resistances,  $R_1$  and  $R_2$ . The Thevenin equivalent voltage from Figure 6.4 (b) is given as

$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

Thevenin equivalent resistance  $R_{th}$  is given as

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

The modified Thevenin equivalent circuit of the potential divider bias circuit is given in Figure 6.4 (b).

Applying KVL on the input loop,

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$V_{th} = V_{BE} + I_B R_{th} + (I_C + I_B) R_E$$

$$V_{th} = V_{BE} + I_B (R_{th} + R_E) + I_C R_E \quad (4)$$

Applying KVL on the output loop,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

Since  $I_C \approx I_E$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

## NOTES

Stability factor, S:

$$S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

**NOTES**

$$(4) \Rightarrow V_{th} = V_{BE} + I_B (R_{th} + R_E) + I_C R_E$$

Differentiating the expression (4)

$$0 = 0 + \partial I_B (R_{th} + R_E) + \partial I_C R_E \frac{\partial I_B}{\partial I_C} = - \frac{R_E}{R_{th} + R_E}$$

Therefore,

$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_E}{R_{th} + R_E} \right)}$$

This shows that the stability of the self-bias circuit depends on the potential divider resistances and emitter resistance. Further, it is also proved that the self-bias method provides better stability when compared to the other type biasing methods.

Following observations are necessary for the stability factors in the potential divider bias method.

- In the stability factor expression, the resistance ratio  $\frac{R_E}{R_{th} + R_E}$  determines the stability of the system.
- If  $\frac{R_E}{R_{th} + R_E} = 1$ , then the stability factor is 1.
- For  $\frac{R_E}{R_{th} + R_E} = 1$ ,  $R_{th}$  must be zero. Practically,  $R_{th}$  cannot be zero, but can be made as small as possible.
- Also, it is observed that  $\beta$  is insignificant in determining the stability factor S.

Hence for the design of the potential divider bias following are to be noted,

- $R_{th}$  must be very small
- stability factor is close to 1.

**Table 6.1** Comparison of Biasing Circuits

Transistor Biasing

S. No	Parameters	Base resistor or fixed bias method	Collector to base bias method	Voltage divider method
1.	stability	poor	average	Good
2	Circuit complexity	simple	average	More
3	S	$(1 + \beta)$	$\frac{(1 + \beta)}{1 + \beta \left( \frac{R_C}{(R_C + R_B)} \right)}$	$\frac{(1 + \beta)}{1 + \beta \left( \frac{R_E}{R_{th} + R_E} \right)}$
4	$S'$	$-\frac{\beta}{R_B}$	$-\frac{\beta}{R_B + (1 + \beta) R_C}$	$\frac{-\beta}{R_{th} + (1 + \beta) R_E}$
5	$S''$	$\frac{I_C}{\beta}$	$\frac{I_C \{R_C + R_B\}}{[(1 + \beta) R_C + R_B]}$	$\frac{SI_C}{\beta(1 + \beta)}$

## NOTES

### Important Formula:

- stability factors:

$$S = \frac{\partial I_C}{\partial I_{CO}} \text{ at constant } V_{BE}, \beta.$$

$$S' = \frac{\partial I_C}{\partial V_{BE}} \text{ at constant } I_{CO}, \beta.$$

$$S'' = \frac{\partial I_C}{\partial \beta} \text{ at constant } I_{CO}, V_{BE}.$$

$$S = \frac{(1 + \beta)}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

- Fixed bias method:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B$$

$$S = \frac{\partial I_C}{\partial I_{CO}} = (1 + \beta) \quad S' = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\beta}{R_B} \quad S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C}{\beta}$$

- Collector base bias method:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C}$$

**NOTES**

$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_C}{R_C + R_B} \right)}$$

$$S' = -\frac{\beta}{R_B + (1 + \beta) R_C} \quad S'' = \frac{I_C \{R_C + R_B\}}{[(1 + \beta) R_C + R_B]}$$

- Self-bias or potential divider bias:

$$V_{th} = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{CE} = V_{CC} + I_C (R_C + R_E)$$

$$S = \frac{(1 + \beta)}{1 + \beta \left( \frac{R_E}{R_{th} + R_E} \right)}$$

$$S' = \frac{-\beta}{R_{th} + (1 + \beta) R_E}$$

$$S'' = \frac{S I_C}{\beta (1 + \beta)}$$

**Check Your Progress**

1. Define Biasing.
2. On which factors, stability factor depends?
3. What are the different methods of biasing?

**6.3 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS**

1. Biasing is a process of making the transistor operate satisfactorily as an amplifier by providing external DC bias voltage and circuitry.
2. Stability factors depend on the collector current,  $I_C$ , collector current due to minority carriers,  $I_{C0}$ , the current gain parameter,  $\beta$  and the base-emitter voltage  $V_{BE}$ .

3. The transistor can be biased by the following methods.

- (i) Fixed bias method or base resistor method
- (ii) Collector base bias method
- (iii) Self-bias or potential divider bias

## NOTES

### 6.4 SUMMARY

- The process of making the transistor operate within the active region by providing external circuitry and voltage is called biasing.
- The operating point tends to shift or oscillate between different regions due to the variation of the collector current  $I_C$  and  $\beta$ .
- Stability factors depend on the collector current,  $I_C$ , collector current due to minority carriers,  $I_{C0}$ , the current gain parameter,  $\beta$  and the base-emitter voltage  $V_{BE}$ .
- Biasing may be of following types:
  - (i) Fixed bias method or base resistor method
  - (ii) Collector base bias method
  - (iii) Self-bias or potential divider bias
- The difference between the fixed bias circuit and the collector base bias circuit is that the base resistor is connected to the collector terminal rather than to the supply voltage terminal. This slight change improves the stability factor considerably.

### 6.5 KEY WORDS

- **Transistor biasing:** It is process of applying DC operating current or voltage conditions to the optimum level so that applied AC input signal can be amplified correctly.
- **Stability factor:** It is a measure of the change in collector current with changes in reverse saturation current, is approximately  $\beta + 1$ .
- **Operating point:** It is the DC voltage or current at a specified terminal of a transistor with no input signal applied.



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## 6.6 SELF ASSESSMENT QUESTIONS AND EXERCISES

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### NOTES

#### Short Answer Questions

1. Define biasing.
2. Define stability factor in transistors.
3. What are the different type of stability factors?
4. Mention the different type of biasing methods for transistors
5. Mention the stability factor of the fixed bias method.
6. Mention the stability factor of collector bias method.
7. Mention the stability factor of the self-bias method.
8. Compare the biasing methods for transistor.

#### Long Answer Questions

1. Derive the general expression for stability factor in transistors.
2. Explain in detail the fixed bias method of biasing a transistor.
3. Explain in detail the collector bias method of biasing a transistor.
4. Explain in detail the self-bias method of biasing a transistor.

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## 6.7 FURTHER READINGS

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- Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.
- Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.
- Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.
- Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

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# UNIT 7 TRANSISTOR AUDIO POWER AMPLIFIER

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*Transistor Audio  
Power amplifier*

## NOTES

### Structure

- 7.0 Introduction
- 7.1 Objectives
- 7.2 Push-Pull Class B Amplifier
- 7.3 Transformer Coupled Audio Power Amplifier/ Tuned Amplifiers
- 7.4 Answers to Check Your Progress Questions
- 7.5 Summary
- 7.6 Key Words
- 7.7 Self Assessment Questions and Exercises
- 7.8 Further Readings

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## 7.0 INTRODUCTION

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In this unit, you will learn about the two important applications of the transistors, push pull amplifiers of class B type and tuned amplifiers. Both the amplifiers have a specific application. Tuned amplifiers work only at a pre-designed tuned frequency. Class B push-pull amplifiers, on the other hand, were designed to overcome the disadvantages of class A push-pull amplifiers.

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## 7.1 OBJECTIVES

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After going through this unit, you will be able to:

- Discuss the disadvantages of class A push-pull amplifier
- Explain Class B Push-Pull Amplifier
- Explain the working of tuned amplifier

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## 7.2 PUSH-PULL CLASS B AMPLIFIER

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Similar to class A push-pull amplifiers discussed earlier, class B push-pull amplifier also employs complementary transistors connected back to back. The disadvantages of class A push-pull amplifiers include the following:

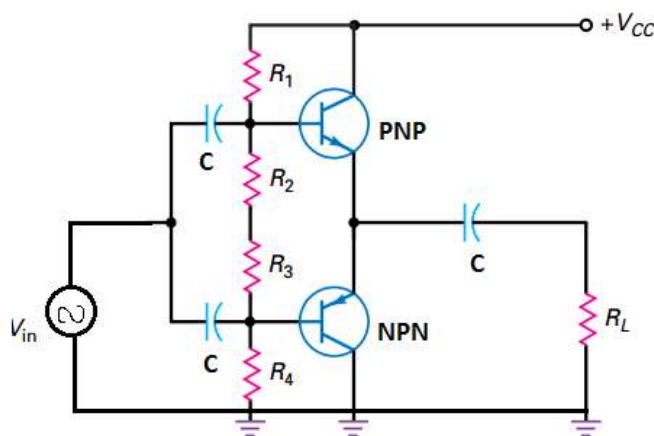
- They are bulky due to the presence of transformers
- They are costlier
- They occupy more space.
- They can't be easily fabricated into ICs

## NOTES

- Their efficiency is less.
- Their cost to operating efficiency ratio is very small

In order to overcome the disadvantages of class A push-pull amplifiers, class B push-pull amplifiers as shown in Figure 7.1 is designed. These amplifiers do not employ any transformers. They consist of two complementary transistors PNP and NPN connected back to back, that is both the emitters are connected to each other. The PNP transistors push the output voltage  $V_{out}$ , to a maximum  $V_{CC}$  voltage and the NPN transistors pulls to minimum ground voltage. These two transistors helps a full output voltage swing between  $+V_{CC}$  to  $GND$  potential. The coupling capacitors connected on the input and the output sides help avoiding the unwanted DC signals entering the amplifier. Resistors  $R_1, R_2, R_3$  and  $R_4$  help the circuit working in the properly biased active region of both the transistors. Resistors  $R_1$  and  $R_2$  help in the biasing of PNP transistor and the resistors  $R_3$  and  $R_4$  help in the biasing of the NPN transistor.

The Class B configuration can provide better power output and has higher efficiency (up to 78.5%). The transistors are biased at the cut-off point and hence they consume no power during idle condition and this adds to the efficiency. The advantages of Class B push-pull amplifiers are, ability to work in limited power supply conditions (due to the higher efficiency), the absence of even harmonics in the output, simple circuitry when compared to the Class A configuration etc. The disadvantages are a higher percentage of harmonic distortion when compared to the Class A push-pull amplifiers, cancellation of power supply ripples is not as efficient as in Class A push-pull amplifier and which results in the need of a well-regulated power supply.



**Fig. 7.1** Class B Push-Pull Amplifier

### 7.3 TRANSFORMER COUPLED AUDIO POWER AMPLIFIER/ TUNED AMPLIFIERS

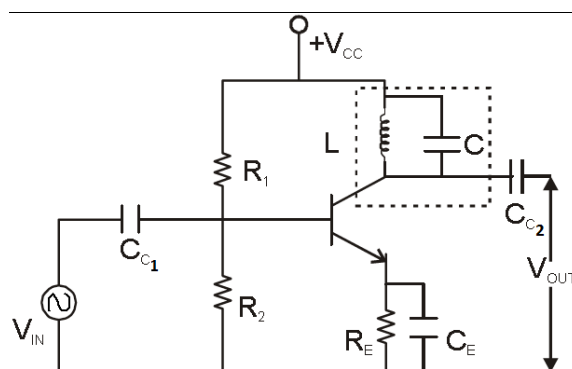
Transistor Audio  
Power amplifier

The amplifier circuit in which, the previous stage is connected to the next stage using a coupling transformer, is known as **Transformer coupled amplifier**. Amplifiers that amplify the input signal only at a tuned frequency are called as tuned amplifiers. In such type of amplifier circuits, amplification is carried out only in a small range of frequencies.

The collector resistances in amplifier circuit is replaced with a tuned or a tank circuit consisting of inductor and capacitor connected in parallel. The charge between the inductor and capacitor keep charging and discharging between them indefinitely. The tuned amplifiers respond well at a resonant frequency. The resonant frequency is a frequency at which the reactance of the circuit cancel each other and the circuit behaves purely as a resistive circuit.

A simple tuned amplifier circuit is shown in Figure 7.2. The tuned circuit consists of the coupling capacitors  $C_{C1}$  and  $C_{C2}$ . The coupling capacitor  $C_{C1}$  in the input side of the amplifier stops the entry of dc signals into the amplifier circuit. Similarly, the coupling capacitor connected in the output side of the amplifier does not allow DC signals from entering back to the collector terminal of the amplifier. The capacitor connected to the emitter terminal in parallel with the emitter resistance  $R_E$  is known as a bypass capacitor. The bypass capacitor  $C_E$  bypasses any unwanted spurious high frequency noise signals arising out of the emitter terminal of the transistor.

The operating frequency of the transistor is tuned by proper choice of the inductor,  $L$  and capacitor,  $C$  values of the tuned circuits. The potential divider resistances  $R_1$  and  $R_2$  ensures the operating point of the amplifier is in the active region. The tuned amplifier circuit described in Figure 7.2 has a potential divider bias tuned LC amplifier.



**Fig. 7.2** Tuned Amplifier

#### NOTES

## NOTES

Under a limiting condition, the bandwidth and resonant frequency of a tuned amplifier is given as:

$$BW = \frac{1}{2\pi RC}$$

$$\text{Resonant Frequency, } f_r = \frac{1}{2\pi\sqrt{LC}}$$

### Advantages of Tuned Amplifiers

The following are the advantages of tuned amplifiers.

- The usage of reactive components like L and C minimizes the power loss, which makes the tuned amplifiers efficient.
- The selectivity and amplification of desired frequency are high, by providing a higher impedance at the resonant frequency.
- A smaller collector supply  $V_{CC}$  would do, because of its little resistance in the parallel tuned circuit.

### Check Your Progress

1. Write any two disadvantages of class A push-pull amplifier.
2. Define tuned amplifier.

## 7.4 ANSWERS TO CHECK YOUR PROGRESS QUESTIONS

1. Two disadvantages of class A push-pull amplifiers are:
  - (i) They are bulky due to the presence of transformers.
  - (ii) They are costlier.
2. Amplifiers that amplify the input signal only at a tuned frequency are called as tuned amplifiers.

## 7.5 SUMMARY

- Class B push-pull amplifiers do not employ any transformers. They consist of two complementary transistors PNP and NPN connected back to back, that is both the emitters are connected to each other.
- The Class B configuration can provide better power output and has higher efficiency (up to 78.5%). The transistors are biased at the cut-off point and hence they consume no power during idle condition and this adds to the efficiency.

- Amplifiers that amplify the input signal only at a tuned frequency are called as tuned amplifiers. In such type of amplifier circuits, amplification is carried out only in a small range of frequencies.
- The operating frequency of the transistor is tuned by proper choice of the inductor, L and capacitor, C values of the tuned circuits.

*Transistor Audio  
Power amplifier*

## NOTES

### 7.6 KEY WORDS

- **Push–pull amplifier:** It is an electronic circuit that uses a pair of active devices that alternately supply current to, or absorb current from, a connected load.
- **Tuned amplifier:** It is an amplifier which uses band pass filtering components within the amplifier circuitry and operates at the selected frequencies.

### 7.7 SELF ASSESSMENT QUESTIONS AND EXERCISES

#### Short Answer Questions

1. Define tuned amplifiers.
2. What do you understand by push-pull amplifiers?
3. Mention the disadvantages of class A push-pull amplifiers.
4. Mention the need for potential divider resistances in amplifier circuits.

#### Long Answer Questions

1. Explain the working of class B push-pull amplifiers with the help of circuit diagram.
2. Explain the working of tuned amplifiers.

### 7.8 FURTHER READINGS

Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

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**BLOCK - III**  
**OPTOELECTRONIC DEVICES AND OSCILLATORS**

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**NOTES**

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**UNIT 8 FIELD EFFECT  
TRANSISTORS AND  
SILICON CONTROLLED  
RECTIFIER**

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**Structure**

- 8.0 Introduction
- 8.1 Objectives
- 8.2 Field Effect Transistor
  - 8.2.1 Types of FET
  - 8.2.2 N-Channel FET
  - 8.2.3 P-Channel FET
  - 8.2.4 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
- 8.3 Silicon Controlled Rectifiers
  - 8.3.1 Working of SCR
  - 8.3.2 Characteristics of Silicon Controlled Rectifiers
- 8.4 Answers to Check Your Progress
- 8.5 Summary
- 8.6 Key Words
- 8.7 Self Assessment Questions and Exercises
- 8.8 Further Readings

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**8.0 INTRODUCTION**

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In this unit, you will learn about the construction, working and analysis of another type of transistors known as field effect transistors. The BJT transistor discussed in an earlier chapter was a current controlled device. BJTs suffer from a disadvantage of lower scalability, lower input impedance etc., hence, field effect transistors abbreviated, as FETs are preferred. The conduction in field effect transistors is due to single charge carriers, unlike the BJTs where the conduction is due to both majority and minority charge carriers. You will also learn about the silicon controlled transistor.

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**8.1 OBJECTIVES**

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After going through this unit, you will be able to:

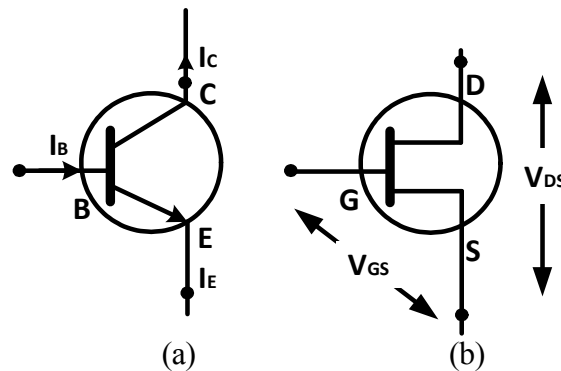
- Explain the construction and working of FET, JFET and MOSFET
- Understand the I/O characteristics of FET

- Explain the construction and working of SCR
- Discuss the characteristics of SCR
- Explain SCR as rectifier

## NOTES

### 8.2 FIELD EFFECT TRANSISTOR

Similar to BJTs, field effect transistors also have three terminals known as a source, drain, and gate. Source terminal is the input terminal, the drain terminal is the output terminal and the gate terminal is the control terminal. The terminals of field effect transistors can be compared to that of water tap terminals. The source is analogous to a water source, tap knob is analogous to the gate terminal and the water discharge is analogous to the drain terminal of FET.



**Fig. 8.1** Circuit Symbol of BJT and FET

As shown in Figure 8.1, the BJTs terminals are base, emitter and collector marked as B, E, and C respectively. Similarly, the terminals of field effect transistors are marked as G, S, and D for the gate, source and drain respectively.

#### FET as Voltage Controlled Device

BJT, as discussed in the earlier chapter, is a current controlled device. The current flow between the emitter terminal and the collector terminal is controlled by the current in the base terminal. In field effect transistors, the flow control between the source and the drain terminal is controlled by the control voltage applied between the gate and source terminal represented as a gate-source voltage,  $V_{GS}$ . The voltage applied between the terminals create an electric field that either enhance or restrict the flow of current. Similarly, the voltage between the drain terminal and source terminal,  $V_{DS}$  determines the magnitude of the current flowing between the two terminals.

Since the electric field controls the flow of current, these devices are called as field effect transistors.



## NOTES

Unlike BJT field effect transistors are unipolar devices. In BJTs the current flow is due to both the majority carriers and the minority carriers, whereas in FETs the current flow is only through the majority carriers which may either be electrons or holes.

FETs are attractive than BJTs because

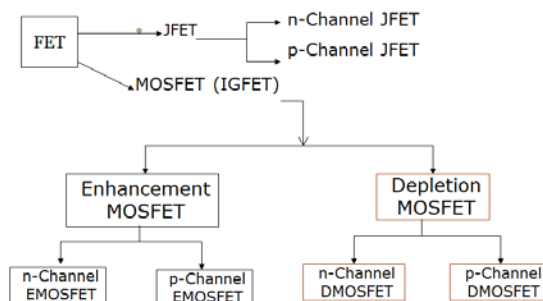
- They offer very high input impedance which is an important property of amplifiers
- They are easily scalable that makes them attractive for fabrication
- They provide more stable operation
- They provided a complete voltage swing between the maximum output voltages.
- The terminals are interchangeable
- They are less noisy when compared to BJTs

### 8.2.1 Types of FET

Field effect transistors are of three types.

1. **Junction Field Effect Transistors (JFETs)**
2. **Metal Oxide Field effect Transistors (MOSFETs)**
3. **Metal Semiconductor Field Effect Transistors (MESFETs)**

FETs are further classified as shown in Figure 8.2.



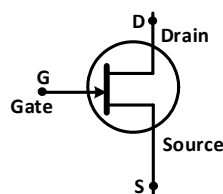
**Fig. 8.2** Classification of FET

The JFETs are classified as non-inverting –channel JFET and P-channel JFET based on the formation of the type of channel between the source and drain.

MOSFETs are also known as **Insulated Gate Field Effect Transistors (IGFETs)**. In MOSFETs, the gate is insulated from the substrate with the help of a dielectric and hence the name IGFET. MOSFETs are also classified as enhancement and depletion mode MOSFETs based on the type of channel formation. Enhancement and depletion mode MOSFETs are further classified as either P-channel type or N–channel type.

### 8.2.2 N-Channel FET

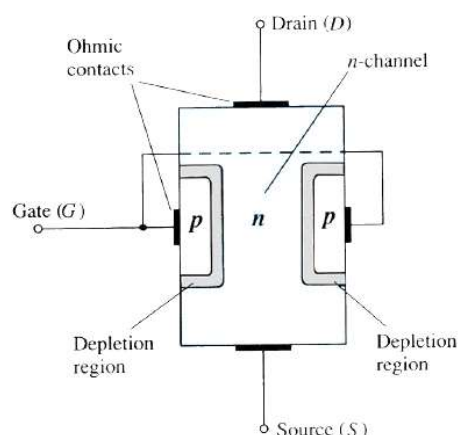
The N-channel JFET has an N-channel FET-type channel between the source and drain. The circuit symbol of N-channel FET is shown in Figure 8.3. In an N-channel FET, the arrowhead at the gate terminal points towards the vertical line which is analogous to the channel.



**Fig. 8.3** Circuit Symbol of N-Channel FET

### Construction of N-Channel FET

The internal cross-section of the N-channel FET is shown in Figure 8.4. The substrate material is made of an extrinsic semiconductor with an N-type material. The terminals source and drain are connected to the substrate material through ohmic contacts. A heavily doped P-type material is fabricated on the sides of the substrate material as shown in Figure 8.4. Two junctions are formed between the P-type and N-type material on either side of the substrate. These junctions are the depletion layer junctions similar to the depletion layer formed in PN junction diodes. The gap between the two depletion layers forms the channel between the source and drain terminals. Same gate potential is applied to both the sides of the P-type material as shown in the figure.



**Fig. 8.4** Construction of N-Channel FET

### Working of N-Channel JFET

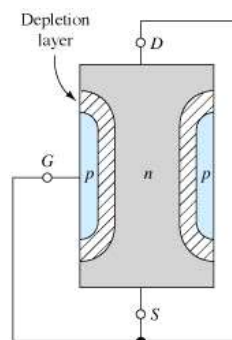
The working of JFET is best understood, by applying the voltage bias to each terminal at once and observing the behavior of the depletion region. Hence, in the first section, gate-source bias is explained.

## NOTES

## NOTES

**(i) Gate-source bias:** Initially, in this section, a bias potential between the gate and the source terminal is applied and the potential between source and drain is kept at 0V. The bias applied is the gate-source voltage. With the terminals open, the gate-source terminals form two p-n junction diodes on either side of the substrate.

**Bias Zero operation:** In the bias zero condition, the gate-source voltage,  $V_{GS} = 0V$ . The terminals between gate and source are short circuited as shown in Figure 8.5.

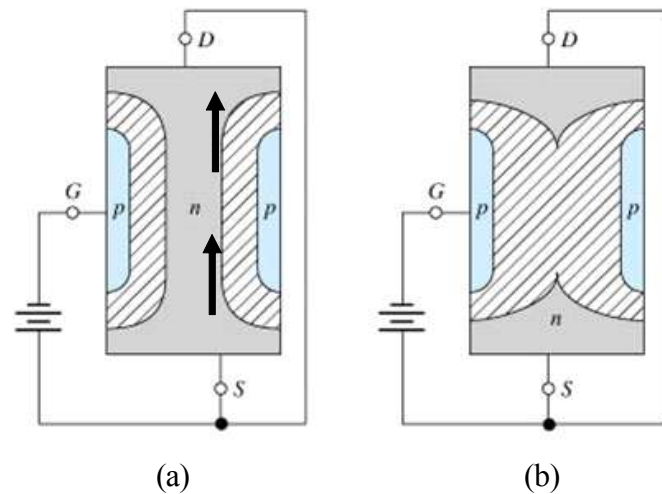


**Fig. 8.5** Zero Bias N-Channel FET

The terminals are at the same potential and hence the depletion layer width around the PN junction is thin and constant. Since the depletion region is very thin, the current conduction between the sources and drain experiences less resistance since the channel area is large. The resistance of the path is inversely proportional to the area of the channel.

$$R \propto \frac{1}{a}$$

**Negative bias operation:** The gate-source voltage,  $V_{GS}$  is supplied such that the PN junction between the gate and the source terminals are reverse biased. A negative source gate voltage is applied. When  $V_{GS}$  is increased, it reverse biases the junction more and the depletion region grows as shown in Figure 8.6 (a). on further increasing the  $V_{GS}$  to larger voltage, the depletion region from both the sides meet each other and gets diffused as observed in Figure 8.6 (b). From Figure 8.6, as the size of the depletion region increases, the area of the channel decreases and hence the resistance offered by the path for the flow of current between the source and drain increases.

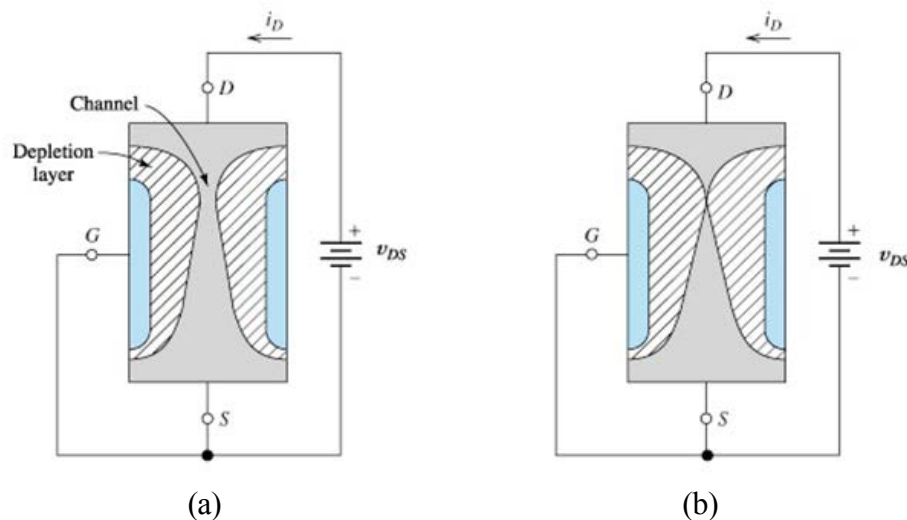


**Fig. 8.6** Negative Bias N-Channel FET

Since the width of the channel is similar on all sides, the resistance offered also is constant throughout the path of flow of charge carriers. Since the channel is a P-type channel, the majority carriers are electrons and the conduction is due to only electrons. This flow of electrons constitutes the drain current  $I_D$ .

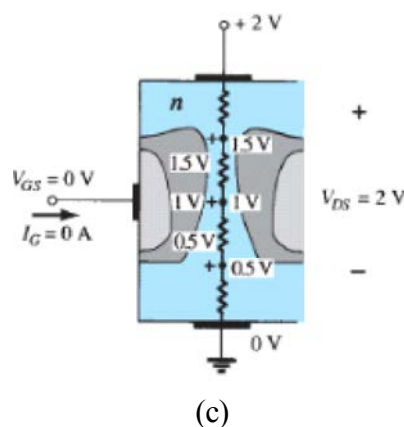
When the gate-source reverse bias voltage is larger such that the depletion region from both the sides diffuse each other, the current flow between the source and drain becomes constant.

**(ii) Source-drain bias:** In this bias condition, the voltage between the source and drain  $V_{DS}$  is applied. The voltage  $V_{DS}$  is applied such that, it aids the conventional current to flow from drain to source and it reverse biases the n-p junction. When voltage  $V_{DS}$  is applied the gate source voltage,  $V_{GS}$  is shorted, that is  $V_{GS} = 0V$ .



## NOTES

## NOTES



**Fig. 8.7** Source Drain Bias for (a)  $V_{DS} > 0$ , (b) Pinch Off for  $V_{DS} \gg 0$ , (c) Internal Potential Divider for JFET

When a voltage,  $V_{DS}$  is applied, the drain terminal is higher potential than the source terminal. The electrons from the source terminal moves towards the drain terminal. According to conventional current flow, current flows from drain to source as shown in Figure 8.7 (a). Also, since the drain potential is higher than the source potential due to the application of  $V_{DS}$  voltage, the depletion layer nearer to the drain terminal is more reverse biased than the depletion layer closer to the source terminal. Hence, the depletion layer resembles similar to as shown in Figure 8.6 (a). Therefore, the resistance offered by the channel path for the flow of current is also different from one point to the other in the channel region. The resistance nearer to the source terminal is less, whereas near the drain terminal, the resistance is high. The channel nearer to the drain terminal offers a larger potential difference than the source terminal. Hence, the JFET can be visualized having internal potential divider circuit as shown in Figure 8.7 (c).

On further increasing the  $V_{DS}$  to a much large value, the two depletion layer on both the sides will meet as shown in Figure 8.6 (b) nearer to the drain terminal. The voltage  $V_{DS}$  at which the two depletion layer meets is known as **pinch off voltage**,  $V_p$ . The electron flow after the pinch off condition becomes stable and a constant drain current,  $I_D$  flows.

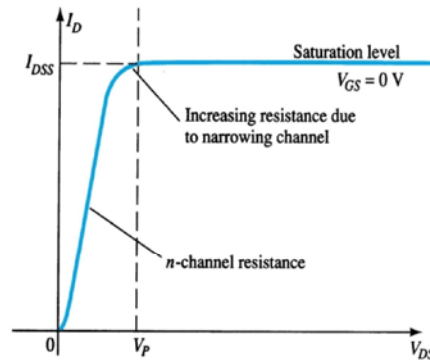
### Characteristics of N-Channel JFET

The working of N-channel JFET described in the previous section is depicted in the operating characteristics as shown in Figure 8.8. As evident from the characteristics, with  $V_{GS} = 0V$ , when  $V_{DS}$  is increased, the drain current,  $I_D$  increases linearly. At this stage, the depletion region width keeps growing and at the same time due to the growing potential difference between the drain and the

source terminal current also increases linearly. The slope of the linearly increasing characteristics provide the channel resistance of the JFET. The slope is given as

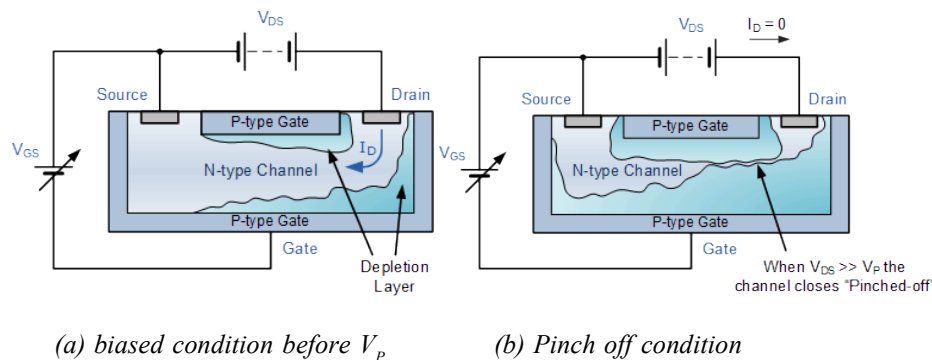
$$R_{ch} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{\text{Change in } V_{DS}}{\text{Change in } I_D}$$

When  $V_{DS} < V_P$ , for a small change in  $V_{DS}$ , there is a very large change in  $I_D$  and hence the resistance of the channel is small. As  $V_{DS} \approx V_P$ , for a small change in  $V_{DS}$ ,  $I_D$  also experiences a small change, indicating the increase in resistance. Once pinch off occurs, the current remains constant. It should be observed that, diffusion of depletion layer do not cause the current flow to stop. Since the structure is a three-dimensional structure, there continue to exist a small path for the flow of current and the current remains constant as  $V_{DS} > V_P$ .



**Fig. 8.8** Characteristics of N-Channel JFET ( $V_{GS} = 0V$ )

The above explanation holds good for  $V_{GS} = 0V$ . Now, when the gate source voltage is applied to a more negative voltage, the applied voltage augments the reverse biased depletion region. The biasing is as provided in Figure 8.9.

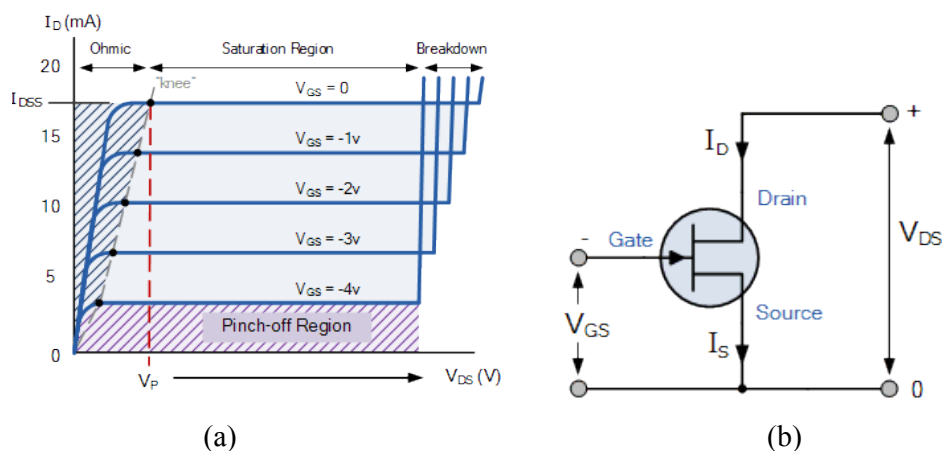


**Fig. 8.9** Three-dimensional Structure of N-Channel FET

## NOTES

## NOTES

For a  $V_{GS} < 0$ , (or  $V_{SG} > 0$ ) more negative voltage is applied to the PN junction between the gate and the source terminal. Pinch off occurs much earlier than when compared to  $V_{GS} = 0V$ . For  $V_{GS} \ll 0V$ , the characteristics shifts downwards as shown in Figure 8.10. when  $V_{GS}$  becomes more negative, the drain current reduces and for a much large negative voltage of  $V_{GS}$ , the depletion region blocks the path of flow of current between the source and drain on the third dimensional side also. Hence, the N-channel JFET stops conducting and reaches a cut-off/pinch-off region. The complete characteristics of N-channel JFET is shown in Figure 8.10.



**Fig. 8.10** (a) Characteristics of N-Channel FET (b) Circuit Representation of JFET Biasing

When  $V_{DS} \gg V_P$ , the breakdown of the channel occurs. The  $v-i$  characteristics of the N-channel JFET is divided into four regions.

- (i) Ohmic region
- (ii) Saturation region
- (iii) Pinch off or cut off region
- (iv) Breakdown region

**Ohmic Region** – When  $V_{GS} = 0$  the depletion layer of the channel is very small and the JFET acts like a *voltage controlled resistor*.

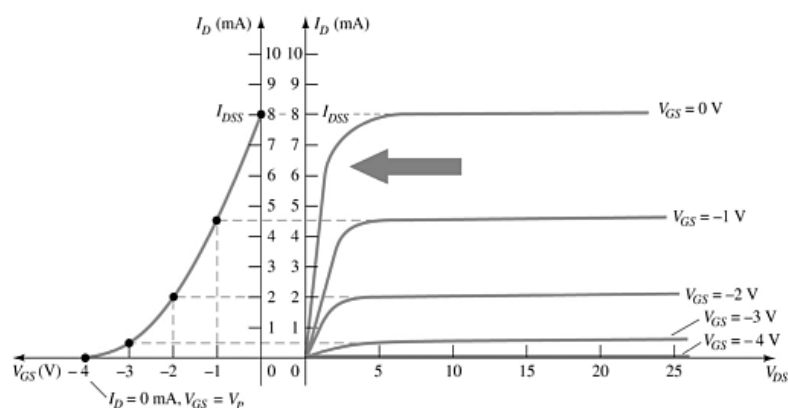
**Cut-off Region** – This is also known as the pinch-off region where the Gate voltage,  $V_{GS}$  is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.

**Saturation or Active Region** – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, ( $V_{GS}$ ) while the Drain-Source voltage, ( $V_{DS}$ ) has little or no effect.

**Breakdown Region** – The voltage between the Drain and the Source, ( $V_{DS}$ ) is high enough to cause the JFET's resistive channel to break down and pass uncontrolled maximum current.

### Transfer Characteristics of JFET

Transfer characteristics are the characteristics plotted between the output parameter and the input parameter. In JFET, the input parameter is the controlling voltage,  $V_{GS}$  and the output parameter is the output current  $I_D$ . Transfer characteristics is plotted from the  $v-i$  characteristics as shown in Figure 8.11



**Fig. 8.11** Transfer Characteristics of N-Channel FET

The transfer characteristics relate to input and output variables. Mathematically, using Shockley's equation, the transfer characteristics can be expressed as:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

Where  $I_{DSS}$  = saturation drain current

The transfer characteristics is a nonlinear characteristic which makes it important to have a nonlinear expression. The nonlinearity is implied through the square function for the drain current  $I_D$ .

### Configurations of JFET

Similar to BJT, FETs also have a different mode of a configuration such as

- (i) Common source configuration
- (ii) Common drain configuration
- (iii) Common gate configuration

### NOTES

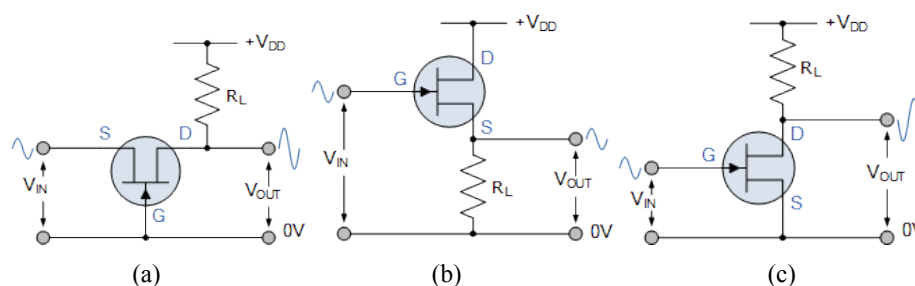


## NOTES

In the **Common Source configuration** (similar to common emitter), the input is applied to the Gate and its output is taken from the drain as shown in Figure 8.12. This is the most common mode of operation of the FET due to its high input impedance and good voltage amplification. Common Source amplifiers are widely preferred for practical use. The common source mode of FET connection is generally used in audio frequency amplifiers and in high input impedance pre-amplifier and cascading stages. Being an amplifying circuit, the output signal is  $180^\circ$  “out-of-phase” with the input.

In the **Common Gate configuration** (similar to common base), the input is applied to the Source and its output is taken from the drain with the gate connected directly to ground as shown. The high input impedance feature of the previous connection is lost in this configuration as the common gate has a low input impedance, but a high output impedance. This type of FET configuration can be used in high-frequency circuits or in impedance matching circuits where a low input impedance needs to be matched to a high output impedance. The output is “in-phase” with the input.

In the **Common Drain configuration** (similar to common collector), the input is applied to the Gate and its output is taken from the Source. The common drain or “source follower” configuration has a high input impedance and a low output impedance and near-unity voltage gain so is therefore used in buffer amplifiers. The voltage gain of the source follower configuration is less than unity, and the output signal is “in-phase”, with the input signal. This type of configuration is referred to as “Common Drain” because there is no signal available at the drain connection, the voltage present,  $+V_{DD}$  just provides a bias. The output is in-phase with the input.



**Fig. 8.12** Different Configuration of FETs (a) Common Source (b) Common Gate (c) Common Drain

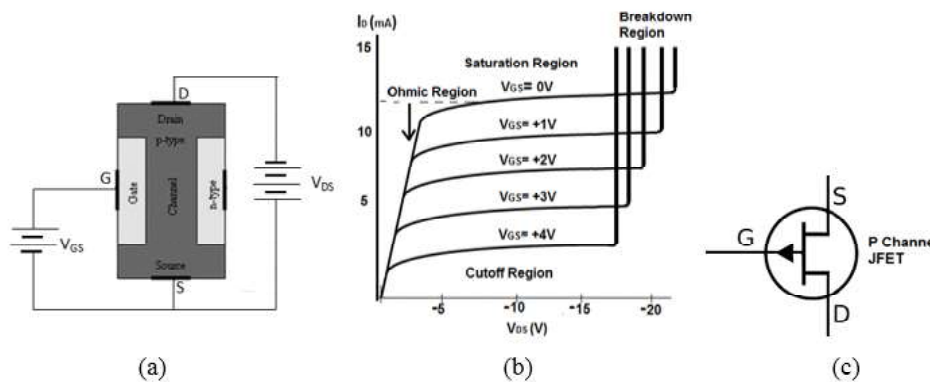
### 8.2.3 P-Channel FET

P-channel FET consists of a P-type substrate connecting the source and the drain terminal. The gate is made of N-type material. The channel thus formed is a P-channel. Both the junctions of gate-source must be reverse biased and hence a positive polarity as shown in Figure 8.13 is given. Similarly, the drain-source voltage

must augment the flow of current from the source and drain and also augment the formation of the depletion layer and hence the potential as shown in Figure 8.13 is connected.

The characteristics will be similar to the N-channel FET except for the polarity of the voltages,  $V_{DS}$  and  $V_{GS}$  are reversed.

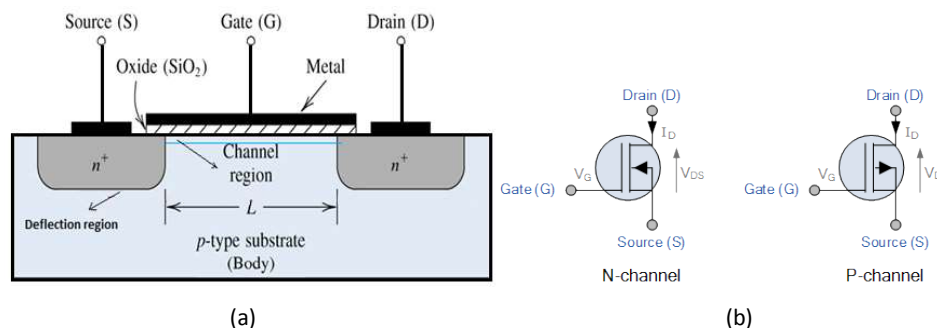
## NOTES



**Fig. 8.13** P-Channel FET (a) Construction (b) V-I Characteristics (c) Symbol

### 8.2.4 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

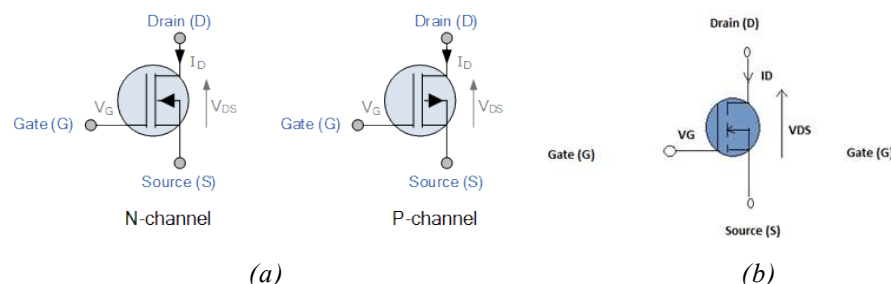
The MOSFETs are another type of FETs that differs from the JFETs by internal construction. MOSFETs also have a channel between the source and drain terminals. But, the source and drain terminals are connected to a single type of heavily doped diffused materials. If the substrate is P-type, the diffusion is by N-type materials and if the substrate is N-type, the diffusion materials are of P-type materials. The important difference between the JFETs and MOSFETs are the way the gate terminal is connected. In MOSFET the gate terminal is insulated from the substrate. MOSFET derived its name from its construction of gate terminal. Gate terminal is a metal terminal followed by an insulator oxide terminal and the substrate forming the semiconductor terminal. The cross-section of MOSFET is as shown in Figure 8.14.



**Fig. 8.14** MOSFET (a) Cross Sectional View, (b) Circuit Symbol

## NOTES

The circuit symbol of MOSFET is also shown in Figure 8.15. For an N-channel MOSFET, the arrowhead points towards the channel line of the circuit symbol. For an N-channel MOSFET, the substrate is of P-type and hence when potential is applied the electrons in the P-type substrate moves towards the gate terminal forming a channel. For a P-channel MOSFET, the arrowhead is away from the channel. The circuit symbol shown in Figure 8.15 (a) is for depletion type MOSFET. For an enhancement type MOSFET, the channel line is broken as shown in Figure 8.15 (b).



**Fig. 8.15** Circuit Symbol (a) Enhancement Type MOSFET, (b) Depletion Type MOSFET

MOSFETs are also known as Metal-Insulator-Semiconductor (MISFET) field effect transistors. The diffused materials are heavily doped and the substrate is lightly doped. The conduction from source to drain takes place through a channel between the two diffused materials either by an existing diffused channel or by an enhanced channel by proper application of potentials.

MOSFETs are classified into two categories based on the type of channels. They are

- (i) Depletion type MOSFET (DMOSFET)
- (ii) Enhancement type MOSFET (EMOSFET)

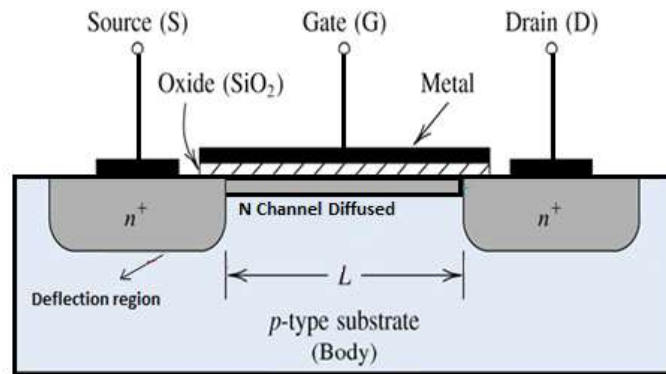
Further depletion type MOSFET and enhancement type MOSFET are classified into N-channel MOSFET and P-channel MOSFET.

### N-Channel Depletion Type MOSFET

#### Construction:

N-channel depletion type MOSFET consists of a lightly doped P-type substrate. The structure is shown in Figure 8.16. The P-type substrate is diffused with two heavily doped N-type material. Through ohmic contacts, the terminals source and drain are connected to the N-type diffusion material. In addition to the N-type diffused material, an n- channel is also diffused to enable the electrons to flow from the source and drain. A dielectric oxide layer is sandwiched between the diffused n- channel and the gate terminal. The oxide layers insulate the gate terminal from the channel. The idea behind the insulation is to avoid the flow of leakage current through the gate and to have a field control of the electrons on the channel

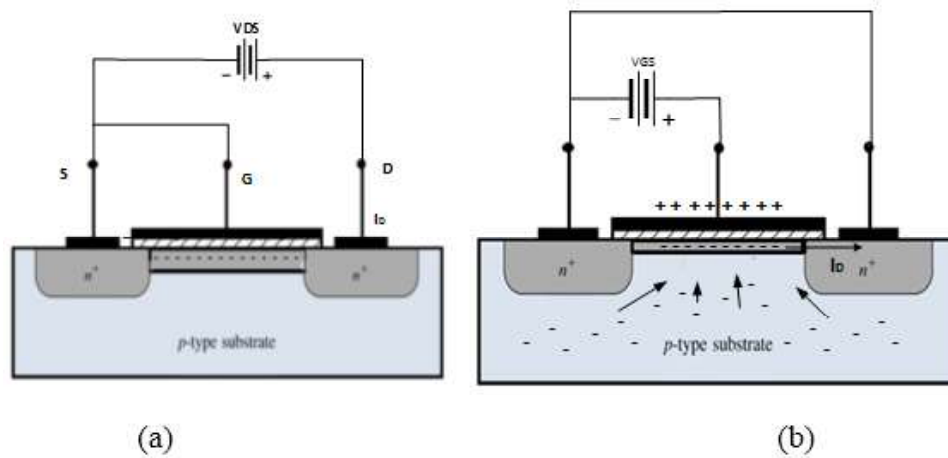
rather than a current controlled channel.



**Fig. 8.16** MOSFET Construction

### Working:

MOSFET is initially applied with zero gate-source voltage, that is  $V_{GS} = 0V$ . Voltage between the drain and the source is applied as shown in Figure 8.17 (a). Drain terminal is at a positive potential and the source terminal is at a negative potential.



**Fig. 8.17** Working of N-Channel MOSFET with (a)  $V_{GS} = 0V$  (b)  $V_{GS} > 0V$   
and  $V_{DS} = 0V$

Since the diffused materials are heavily doped N-type material, the electrons on the source side get deflected by the negative potential and the electrons on the drain side get attracted by the positive potential. When  $V_{DS}$  is increased, the drain is at the higher potential than the source terminal which makes the electrons move from source to drain through the already diffused N-type channel. With increase

### NOTES

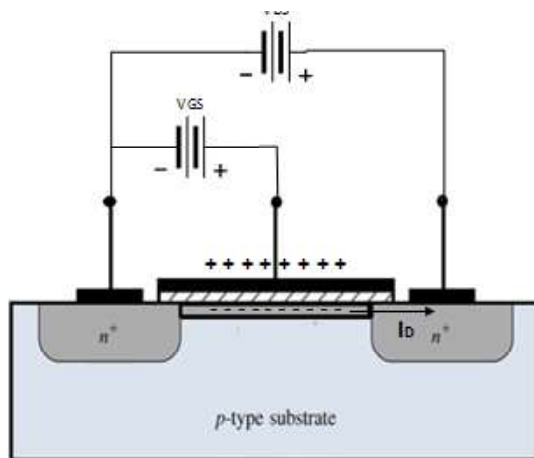
## NOTES

in  $V_{DS}$  continue to increase linearly.

When  $V_{DS} = 0V$  and  $V_{GS} > 0V$  is applied across the DMOSFET, since the gate is insulated from the substrate, the gate terminal and the substrate terminal act like a capacitor and the charges start accumulating on both the sides of the terminals as shown in Figure 8.17 (b). Since the gate terminal is positive, positive charges accumulate on the gate terminal side. The P-type substrate is usually grounded. The positive gate terminal attracts the distributed electrons in the substrate towards the gate terminal. This results in the accumulation of electrons below the oxide layer in the substrate. The accumulation of electrons aids in the formation of a channel for the flow of electrons from source to drain.

When both  $V_{GS} > 0V$  and  $V_{DS} > 0V$ , the gate source voltage  $V_{GS}$  aids in the formation of the channel along with the already existing diffused N-type channel and the  $V_{DS}$  aids in the flow of charges from source to drain. Application of  $V_{GS}$  thus increases the area of the channel. The depletion type MOSFET is normally switched “ON” (conducting) without the application of a gate bias voltage. That is the channel conducts when  $V_{GS} = 0$  making it a “normally-closed” device.

For the N-channel depletion MOS transistor, a negative gate-source voltage,  $V_{GS} < 0V$  will deplete (hence its name) the conductive channel of its free electrons switching the transistor “OFF”. Likewise for a P-channel depletion MOS transistor a positive gate-source voltage,  $V_{GS} > 0V$  will deplete the channel of its free holes turning it “OFF”.



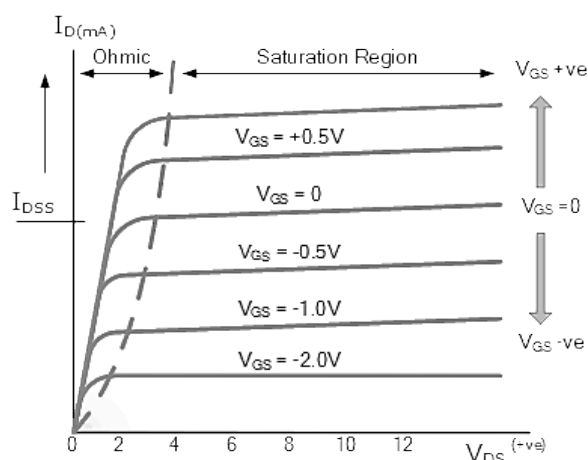
**Fig. 8.18** Working of N-Channel MOSFET with  $V_{GS} > 0V$  and  $V_{DS} > 0V$

In other words, for an N-channel depletion mode MOSFET:  $+V_{GS}$  means more electrons and more current. While a  $-V_{GS}$  means less electrons and less

current. The opposite is also true for the P-channel types. Then the depletion mode MOSFET is equivalent to a “normally-closed” switch.

*Field Effect Transistors and  
Silicon Controlled Rectifier*

### Characteristics of N-Channel MOSFET



**Fig. 8.19** Characteristics of N-Channel Depletion Type MOSFET

The characteristics of N-channel depletion type MOSFET is shown in Figure 8.19. When  $V_{GS}$  is positive, the drain current increases more whereas when  $V_{GS}$  is negative the channel is depleted leading to lesser drain current. MOSFET also exhibits similar characteristics to JFET and BJTs. The characteristics can be divided into four regions, ohmic region, saturation region, breakdown region and cutoff region. When MOSFET is operated in the ohmic region, they are used as resistors and when operated in the saturation region, they are used as amplifiers. When  $V_{GS} < 0V$ , the MOSFET is operating in depletion mode and when  $V_{GS} > 0V$ , the MOSFET is operating in enhancement mode of operation.

### P-Channel Depletion Type MOSFET

P-channel depletion type MOSFET is less preferred due to the mobility of holes. Since the mobility of holes is 3 times less than the electrons, P-channel type devices are rarely used in practice. In P-channel depletion type MOSFET, the polarity is reversed when compared to the N-channel counterpart. When  $V_{GS} > 0V$ , the MOSFET is operating in depletion mode and when  $V_{GS} < 0V$ , the MOSFET is operating in enhancement mode of operation.

### N-Channel Enhancement Type MOSFET

The major difference between the enhancement type MOSFET and depletion type MOSFET is that an enhancement type MOSFET, there doesn't exist a pre diffused channel, whereas, in depletion type MOSFET, a channel is diffused during the fabrication of the device.

### NOTES

## NOTES

Enhancement type MOSFET are classified as P-channel enhancement type and N-channel enhancement type MOSFETs.

The nonexistence of the conducting channel makes this type of MOSFET devices being normally “OFF” (non-conducting) when the gate bias voltage,  $V_{GS} = 0V$ . The circuit symbol shown in figure 8.15 (b) for an enhancement MOS transistor uses a broke N-channel line to signify a normally open non-conducting channel.

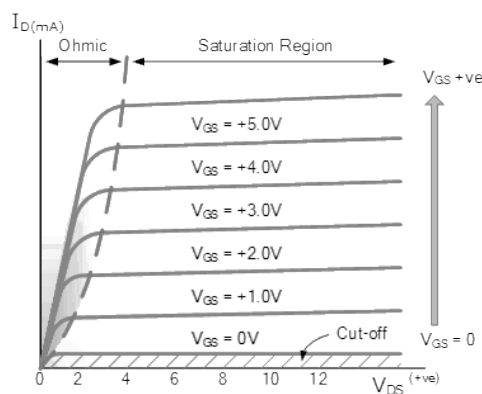
For the N-channel enhancement MOS transistor a drain current will only flow when a gate voltage ( $V_{GS}$ ) is applied to the gate terminal greater than the threshold voltage ( $V_{TH}$ ) level in which conductance takes place making it a transconductance device.

The application of a positive (+ve) gate voltage to an N-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current,  $I_D$  through the channel. In other words, for an N-channel enhancement mode MOSFET:  $+V_{GS}$  turns the transistor “ON”, while a zero or  $-V_{GS}$  turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

The reverse is true for the P-channel enhancement MOS transistor. When  $V_{GS} = 0$  the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the P-type eMOSFET enhances the channels conductivity turning it “ON”. Then for a P-channel enhancement mode MOSFET:  $+V_{GS}$  turns the transistor “OFF”, while  $-V_{GS}$  turns the transistor “ON”.

### Characteristics of N-Channel Enhancement Type MOSFET



**Fig. 8.20** Characteristics of N-Channel Enhancement Type MOSFET

The characteristics of enhancement type MOSFET is shown in figure 8.20. A negative  $V_{GS}$  voltage does not create a channel and hence there doesn't exist a path for the current conduction between the source and drain. This results in the MOSFET operating as a switch in an OFF condition. MOSFET operates in the cutoff mode. When  $V_{GS} > 0V$ , the channel is enhanced and the drain current,  $I_D$  starts to flow from source to drain. When an increase in  $V_{DS}$ , the drain current increases linearly till the threshold voltage, beyond which the drain current saturates. This saturation of the drain current is due to the fact that, the magnitude of the drain current is limited by the width of the channel to accommodate the electron flow. When the channel width is enhanced by more positive  $V_{GS}$  voltage, the drain current also increases.

When  $V_{DS} \gg V_{TH}$ , the breakdown of the MOSFET occurs. This region of operation is the breakdown region of the MOSFET. The linear ohmic region offers a resistive region of operation of the MOSFET to be used as resistive devices.

The MOSFETs ability to change between the two states enables it to have two basic functions: “switching” (digital electronics) or “amplification” (analog electronics). Then MOSFETs have the ability to operate within three different regions:

1. **Cut-Off Region** – with  $V_{GS} < V_{\text{threshold}}$  the gate-source voltage is much lower than the transistors threshold voltage so the MOSFET transistor is switched “fully-OFF” thus,  $I_D = 0$ , with the transistor acting like an open switch regardless of the value of  $V_{DS}$ .
2. **Linear (Ohmic) Region** – with  $V_{GS} > V_{\text{threshold}}$  and  $V_{DS} < V_{GS}$  the transistor is in its constant resistance region behaving as a voltage-controlled resistance whose resistive value is determined by the gate voltage,  $V_{GS}$  level.
3. **Saturation Region** – with  $V_{GS} > V_{\text{threshold}}$  and  $V_{DS} > V_{GS}$  the transistor is in its constant current region and is therefore “fully-ON”. The Drain current  $I_D = \text{Maximum}$  with the transistor acting as a closed switch.

**Table 8.1** The Switching Table of the MOSFET

MOSFET type	$V_{GS} = +ve$	$V_{GS} = 0$	$V_{GS} = -ve$
N-channel Depletion	ON	ON	OFF
N-channel Enhancement	ON	OFF	OFF
P-channel Depletion	OFF	ON	ON
P-channel Enhancement	OFF	OFF	ON

## NOTES



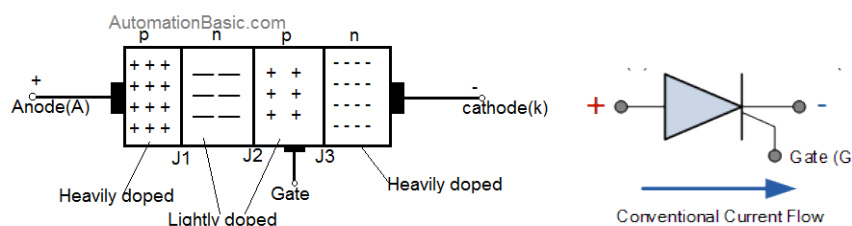
## NOTES

### Check Your Progress

1. What are the three terminals of FET?
2. What are the three types of field effect transistor?

## 8.3 SILICON CONTROLLED RECTIFIERS

Silicon Controlled Rectifiers abbreviated as SCRs are multi-layered transistors used to have a control on the ON condition of the transistor. SCRs are also called as thyristors. Thyatron + transistor is a thyristor. A thyatron is a gas-filled device used in early days that exhibit the same behavior of thyristors. SCRs have three terminals, an anode terminal, a cathode terminal, and the gate terminal. The circuit symbol is as shown in Figure 8.21.



**Fig. 8.21** Silicon Controlled Rectifiers Construction and Circuit Symbol

Silicon controlled rectifiers consists of two PN-PN diodes sandwiched to each other forming PNPN structure. The P and N-type semiconductors on both the end sides of the SCRs are heavily doped, whereas the other two N and P-type semiconductors are lightly doped. The anode is connected to the heavily doped P-type and the cathode is connected to the heavily doped N-type semiconductor. The gate terminal is connected to the lightly doped P-type semiconductor as shown in Figure 8.21. The PNPN SCR consists of three junctions  $J_1$ ,  $J_2$  and  $J_3$ .

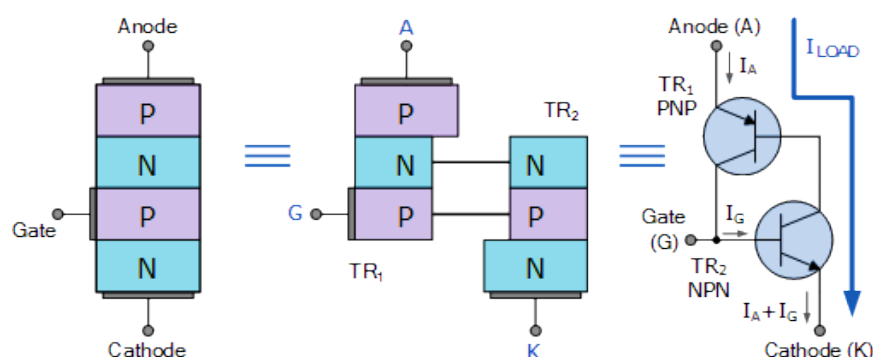
The circuit symbol of the SCR is similar to the diode, but with an additional gate terminal indicating as a controlled diode. Whenever an input pulse is available across the gate terminal, the SCR conducts. Silicon controlled rectifiers even though they are forward biased, does not conduct without the gate input pulse. Once the SCR starts conducting, they are unstoppable and the SCR continues to conduct till the end of the input cycle, i.e., till the polarity reverse biases the SCR.

### Dual Transistor Analogy of SCR

The PNPN structure of SCR can be visualized as two transistors, one with a PNP configuration and the other with an NPN configuration shorted between each other. Consider the PNP transistor as  $T_{R1}$  and the NPN transistor as  $T_{R2}$ . The collector of the PNP transistor is connected to the base of the NPN transistor and

similarly, the collector of the NPN transistor is connected to the base of the PNP transistor. The gate pulse is connected to the base of the NPN transistor. Whenever the gate pulse is presented at the base of the NPN transistor, transistor  $T_{R2}$  is ON, with the collector current triggering the base of  $T_{R1}$ , thereby current conduction takes place between the anode and the cathode. If the anode current is  $I_A$ , the cathode current is the sum of  $I_A$  and the gate current,  $I_G$ .

## NOTES



**Fig. 8.22** Dual Transistor Analogy of SCR

Thus, these two inter-connected transistors rely upon each other for conduction as each transistor gets its base-emitter current from the other's collector-emitter current. So until one of the transistors is given some base current nothing can happen even if an Anode-to-Cathode voltage is present.

### 8.3.1 Working of SCR

When the thyristors anode terminal is negative with respect to the Cathode, the center N-P junction is forward biased, but the two outer P-N junctions are reversed biased and it behaves very much like an ordinary diode. Therefore a thyristor blocks the flow of reverse current until at some high voltage level, leading to the breakdown voltage point of the two outer junctions and thereby the thyristor conducts without the application of a Gate signal.

This is an important negative characteristic of the thyristor, as it can be unintentionally triggered into conduction by a reverse over-voltage as well as high temperature or by a rapidly rising spike voltage.

If the Anode terminal is made positive with respect to the Cathode, the two outer P-N junctions are now forward biased but the center N-P junction is reverse biased. Therefore forward current is also blocked. If a positive current is injected into the base of the NPN transistor  $TR_2$ , the resulting collector current flows in the base of transistor  $TR_1$ . This, in turn, causes a collector current to flow in the PNP transistor,  $TR_1$  which increases the base current of  $TR_2$  and so on.

Very rapidly the two transistors force each other to conduct to saturation as they are connected in a regenerative feedback loop that cannot stop. Once triggered into conduction, the current flowing through the device between the Anode and

## NOTES

the Cathode is limited only by the resistance of the external circuit as the forward resistance of the device when conducting can be very low at less than  $1\Omega$  so the voltage drop across it and power loss is also low.

When an AC voltage is applied to the SCR, it blocks the current flow into the SCR in both the cycles. When the SCR is turned ON with the help of a gate pulse, the SCR works similar to the normal rectifying diode.

### 8.3.2 Characteristics of Silicon Controlled Rectifiers

The characteristics of the silicon controlled rectifiers are shown in Figure 8.23. The applied anode-cathode voltage is the forward voltage of the SCR and the current flowing from anode to cathode is the forward current for the SCR. When a forward voltage is applied between the anode and the cathode terminals, since junctions  $J_1$  and  $J_3$  are forward biased, but the junction  $J_2$  is reverse biased, the forward current is blocked. Hence, the SCR is in the OFF state. There exists a small leakage current that flows for an increase in forward voltage.

However on applying extensive forward voltage, the junction  $J_2$  breaks down at a voltage known as *knee voltage*. Once the junction is broken down, the SCR continues to conduct indefinitely as shown in Figure 8.23. Now, the SCR is said to be turned ON. After the breakdown occurs, the conduction starts abruptly and the current from which the SCR starts to conduct is known as **holding current**. It is to be noted that a gate pulse is not applied during this state of operation.

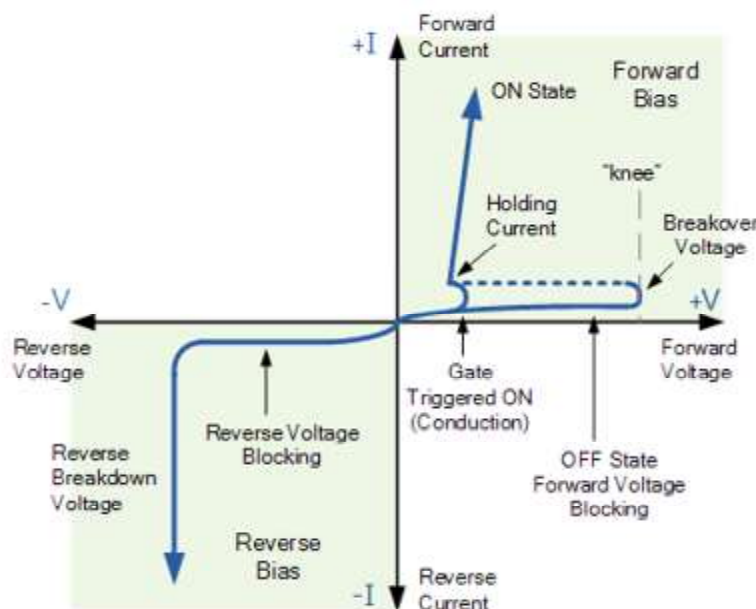


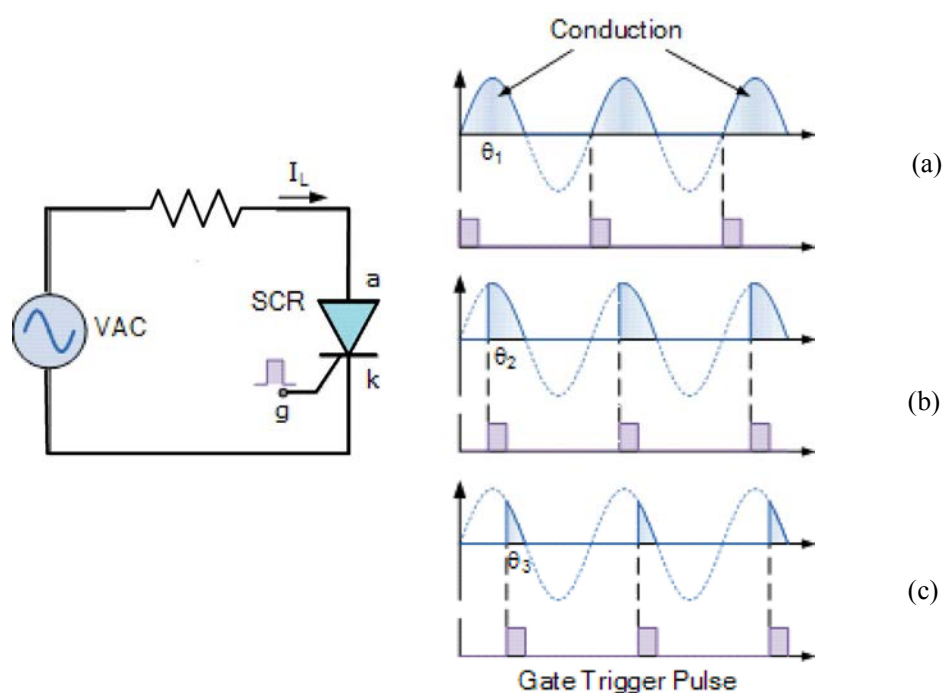
Fig. 8.23 I-V Characteristics of SCR

When the SCR is in the OFF state with a forward voltage less than the knee voltage, when a gate pulse is given at the gate terminal, junction  $J_2$  is forward

biased. This makes the current to flow from anode to cathode. The minimum magnitude of the current beyond which the current starts to flow abruptly in an SCR is known as the holding current. On triggering the gate pulse, the current conduction starts from the holding current magnitude and the thyristor is said to be turned ON.

When a reverse voltage is applied to the thyristor, it behaves similarly to the diode in the reverse biased state. The thyristor in reverse potential state makes the junctions  $J_1, J_3$  reverse biased and junction  $J_2$  forward biased. Thus the thyristor is in the OFF state. It conducts only when a large reverse voltage breaks down the reverse biased junction, such that the minority carriers starts to flow.

### Thyristor as Rectifier



**Fig. 8.24** The Input-Output Waveform of SCR

SCRs act like a normal rectifying diode when an alternating voltage is given and hence the name controlled rectifier. The controlled rectification process is done with the help of the gate pulse triggered at the gate terminal of the SCR. Consider a circuit setup shown in Figure 8.24. An AC supply is supplied to the SCR through a current limiting resistor. The gate pulse is provided at the gate terminals.

The input-output waveforms for SCRs are given in Figure 8.24 (a-c). The gate is triggered at a phase of  $\theta_1, \theta_2$  and  $\theta_3$ . When the triggering angle  $\theta_1 = 0^\circ$ , the input and the output AC waveforms are similar. When the triggering angle

### NOTES

## NOTES

$\theta_1 = 90^\circ$ , the input and the output AC waveforms as shown in figure 8.24 (b) is obtained. The output waveforms appears only after the application of gate triggering pulse. Similarly, the output waveform as depicted in figure 8.24 (c) is obtained when the triggering angle  $\theta_3 > 90^\circ$ . In all the above cases, the SCRs do not conduct in the reverse direction similar to the diode and acts as a controlled half wave rectifier.

### Operating Modes of SCRs

Thyristors have three states which are as follows:

1. **Reverse Blocking Mode** – Voltage is applied in the direction that would be blocked by a diode.
2. **Forward Blocking Mode** – Voltage is applied in the direction that would cause a diode to conduct, but the thyristor has not been triggered into conduction.
3. **Forward Conducting Mode** – The thyristor has been triggered into conduction and will remain conducting until the forward current drops below a threshold value known as the “holding current”.

*Table 8.1 Comparison of FET and BJT*

Sl. No	BJT	FET
1	BJTs are current controlled device.	FETs are voltage controlled device.
2	The terminals are Emitter, base, and collector.	The terminals are Source, gate and drain.
3	They are bipolar devices.	They are unipolar devices
4	There are NPN and PNP-types of transistors.	There are N-channel and P-channel types of FETs.
5	They have CE, CB and CC configurations.	They have CS, CD and CG configurations.
6	They have less input impedance.	They have a high input impedance.
7	They have a high output resistance.	They have a low output resistance.
8	Scaling the transistor results in the change in the operational characteristics.	They are scalable with similar operational characteristics.
9	The gain-BW product is less	They have very high gain-BW product.

### Check Your Progress

3. What are silicon controlled transistors?
4. What is holding current?

### NOTES

## 8.4 ANSWERS TO CHECK YOUR PROGRESS

1. Field effect transistors have three terminals known as a source, drain, and gate.
2. Field effect transistors are of three types.
  - (i) Junction Field Effect Transistors (JFETs)
  - (ii) Metal Oxide Field Effect Transistors (MOSFETs)
  - (iii) Metal Semiconductor Field Effect Transistors (MESFETs)
3. Silicon Controlled Rectifiers abbreviated as SCRs are multi-layered transistors used to have a control on the ON condition of the transistor. SCRs are also called as thyristors.
4. After the breakdown occurs, the conduction starts abruptly and the current from which the SCR starts to conduct is known as holding current.

## 8.5 SUMMARY

- Field effect transistors also have three terminals known as a source, drain, and gate. Source terminal is the input terminal, the drain terminal is the output terminal and the gate terminal is the control terminal.
- In field effect transistors, the flow control between the source and the drain terminal is controlled by the control voltage applied between the gate and source terminal represented as a gate-source voltage,  $V_{GS}$ .
- The JFETs are classified as non-inverting –channel JFET and P-channel JFET based on the formation of the type of channel between the source and drain.
- MOSFETs are also classified as enhancement and depletion mode MOSFETs based on the type of channel formation. Enhancement and depletion mode MOSFETs are further classified as either P-channel type or N–channel type.
- In an N-channel FET, the arrowhead at the gate terminal points towards the vertical line which is analogous to the channel.

## NOTES

- Transfer characteristics are the characteristics plotted between the output parameter and the input parameter. In JFET, the input parameter is the controlling voltage,  $V_{GS}$  and the output parameter is the output current  $I_D$ .
- P-channel FET consists of a P-type substrate connecting the source and the drain terminal. The gate is made of N-type material. The channel thus formed is a P-channel.
- MOSFETs also have a channel between the source and drain terminals. But, the source and drain terminals are connected to a single type of heavily doped diffused materials. If the substrate is P-type, the diffusion is by N-type materials and if the substrate is N-type, the diffusion materials are of P-type materials.
- Silicon controlled rectifiers abbreviated as SCRs are multi-layered transistors used to have a control on the ON condition of the transistor. SCRs are also called as thyristors.
- Silicon controlled rectifiers consists of two PN-PN diodes sandwiched to each other forming PNPN structure.

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## 8.6 KEY WORDS

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- **FET:** It is a transistor that uses an electric field to control the electrical behaviour of the device.
- **MOSFET:** It is a type of field-effect transistor that is usually fabricated by the controlled oxidation of silicon.
- **SCR or Thyristor:** It is a four-layer solid-state current-controlling device.

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## 8.7 SELF ASSESSMENT QUESTIONS AND EXERCISES

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### Short Answer Questions

1. What do you understand by holding current in SCR?
2. What is the difference between the depletion mode and enhancement mode MOSFETs?
3. How is the transfer characteristics in FETs obtained?
4. Draw the circuit symbol of N-channel and P-channel FETs.
5. Draw the circuit symbol of enhancement type MOSFETs and depletion type MOSFETs.
6. Compare FETs and MOSFETs.
7. What is the function of the gate terminal in SCR?

8. Draw the structure of SCR.
9. What are the different operating modes of SCRs?

*Field Effect Transistors and  
Silicon Controlled Rectifier*

### **Long Answer Questions**

1. Explain the construction and working of N-channel FETs.
2. Explain the construction and working of P-channel FETs.
3. Explain the construction and working of depletion type N-channel MOSFETs.
4. Explain the construction and working of enhancement type N-channel MOSFETs.
5. Explain the construction and working silicon controlled rectifiers.

### **NOTES**

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## **8.8 FURTHER READINGS**

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.



## NOTES

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# UNIT 9 POWER ELECTRONICS AND OPTO ELECTRONIC DEVICES

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### Structure

- 9.0 Introduction
- 9.1 Objectives
- 9.2 DIAC
  - 9.2.1 Construction of DIAC
  - 9.2.2 Working of DIAC
- 9.3 TRIAC
  - 9.3.1 Construction of TRIAC
- 9.4 Solar Cells
  - 9.4.1 Working of Solar Cell
  - 9.4.2 Photodetectors
- 9.5 Answers to Check Your Progress
- 9.6 Summary
- 9.7 Key Words
- 9.8 Self Assessment Questions and Exercises
- 9.9 Further Readings

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## 9.0 INTRODUCTION

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In this unit, you will learn about the applications of semiconductor devices in the field of power electronics. Power electronics are electronic devices that are capable of handling high power as against the low power electronic devices such as BJTs and FETs. An extension of silicon controlled rectifiers that was discussed in the last unit is extended to special purpose devices known as DIAC and TRIAC. Additionally, optoelectronic devices such as solar cells that depend on the solar power and the photodetectors will also be discussed in this unit.

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## 9.1 OBJECTIVES

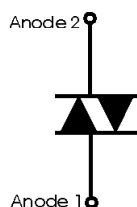
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After going through this unit, you will be able to:

- Understand the construction and working of DIAC and TRIAC
- Explain the working of solar cell
- Discuss the importance and applications of photodetectors

## 9.2 DIAC

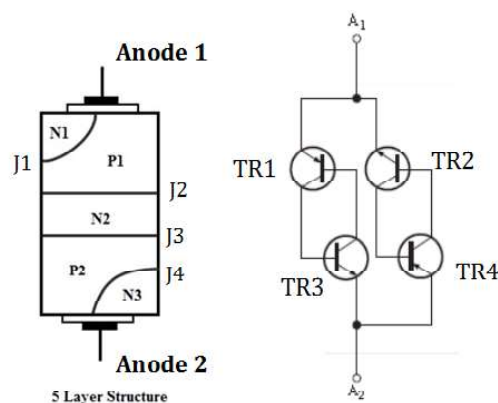
**Diode AC** switch is abbreviated as DIAC. DIAC consists of two terminals Anode 1 and Anode 2. There is no cathode terminal since the two terminals of DIAC can be used interchangeably. The circuit symbol is shown in Figure 9.1. The circuit symbol consists of two triangles connected opposite to each other with the anode terminals.



**Fig. 9.1** Circuit Symbol of DIAC

### 9.2.1 Construction of DIAC

DIAC is a five layer device consisting of N-P-N-P-N structure. Both the N1 and P1 semiconductors are connected to the anode 1 terminal and the semiconductors P2 and N3 are connected to the anode 2 terminal. The five-layer structure can be visualized as a two four-layered structure similar to SCR. The DIAC structure is equivalent to an NPNP (N1P1N2P2) structure looking from the left side of the DIAC and PNP (P1N2P2N3) structure looking from the right side of the DIAC connected back to back. The schematic of the DIAC structure is shown in Figure 9.2 (a).



**Fig. 9.2** (a) Construction of DIAC (b) Equivalent Structure

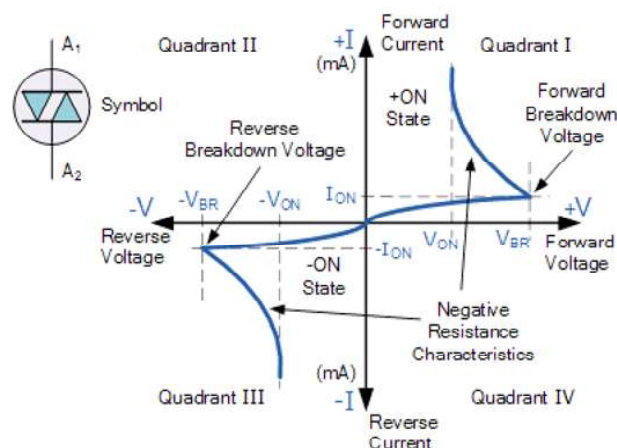
The equivalent circuit diagram for the DIAC structure is given in Figure 9.2 (b). The equivalent structure is similar to the SCR equivalent circuit, where two SCRs are connected back to back, but without the gate terminal. Hence the circuit symbol also resembles the SCR symbol without the gate terminal but connected back to back.

## NOTES

## 9.2.2 Working of DIAC

### NOTES

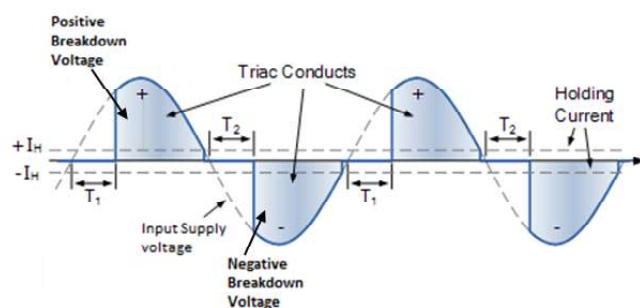
The objective of having such a type of construction with SCRs (without gate) connected back to back is to exploit the advantage of SCR circuit in the reverse direction condition also. When the DIAC is positive biased, i.e. when a voltage  $V_{A1A2}$  is applied across both the terminals, forward characteristics similar to the SCR characteristics is obtained. The DIAC characteristics is shown in Figure 9.3. When a positive biased voltage is applied junctions J2 and J4 are forward biased and junctions J1 and J3 are reverse biased. From the equivalent circuit, transistors TR2 and TR4 are ON, while the transistors TR1 and TR3 are OFF. With junctions J2 and J4 forward biased and junction J3 reverse biased, the forward current conduction is blocked. On increasing the forward voltage to a large magnitude, the forward breakdown of the junction J3 occurs leading to an abrupt increase in the forward current, making the right side equivalent SCR ON. Hence, the characteristics similar to SCR in the first quadrant is obtained.



**Fig. 9.3** V-I Characteristics of DIAC

Similarly, when a negative bias voltage or a reverse voltage is applied between A1 and A2, the junctions J2 and J4 are reverse biased and junctions J1 and J3 are forward biased. From the equivalent circuit, transistors TR2 and TR4 are OFF, while the transistors TR1 and TR3 are ON. With junctions J1 and J3 forward biased and junction J2 reverse biased, the reverse current conduction is blocked. On increasing the reverse voltage to a large magnitude, the reverse breakdown of the junction J2 occurs leading to an abrupt increase in the reverse current, making the left side equivalent SCR ON. Hence, the characteristics similar to SCR in the third quadrant is obtained.

The input-output waveform for a DIAC is shown in Figure 9.4. Unlike SCR, which conducts current only in the positive direction after a breakdown or a gate pulse, DIAC has an advantage of conducting in both the direction after a breakdown. DIAC consists of positive holding current and a negative holding current beyond which the current increase to a larger magnitude.



**Fig. 9.4** The Output Waveform of DIAC

## NOTES

### 9.3 TRIAC

TRIAC is similar to DIAC but with a gate terminal. TRIAC is a three-terminal AC switch. TRIAC is a three terminal, four layer, bidirectional semiconductor device that controls the flow of AC current and AC power in the circuit. It can conduct in both the directions. In DIAC, it was necessary to drive the DIAC to breakdown voltage to make it conduct, but with the presence of gate terminal in TRIAC, the gate pulses may be applied in both the forward and reverse directions to make the TRIAC conduct. TRIAC can be used for AC systems as a controlled switch in both the directions. They are used in control circuits such as switching circuits, phase control circuits for the motor, etc.

#### Circuit Symbol

The circuit symbol of the TRIAC is shown in Figure 9.5 and is similar to the DIAC, but with an additional gate terminal. TRIAC consists of three terminals Anode 1, anode 2 and the gate terminal. Gate terminal is required to provide the triggering gate pulses to the DIAC. The TRIAC symbol is similar to two SCR circuit symbol connected back to back.



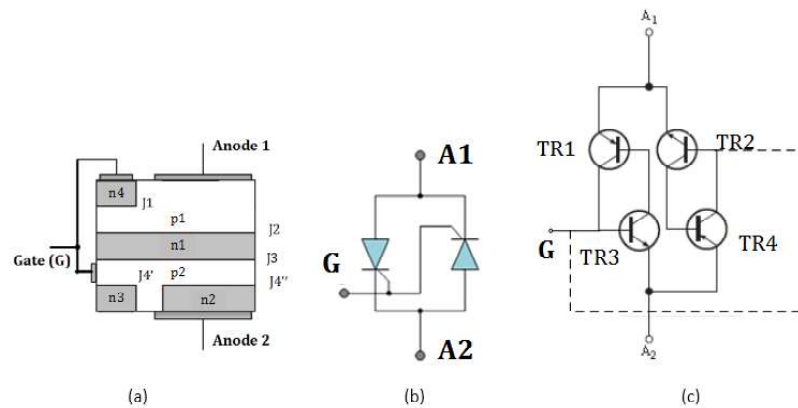
**Fig. 9.5** Circuit Symbol of TRIAC

#### 9.3.1 Construction of TRIAC

The TRIAC consists of two P-type material and four N-type material as shown in Figure 9.6 (a). Semiconductors n3 and p2 are connected to the gate terminal. The gate pulse alters the conduction of the junctions  $J_1$  and  $J_3$ . Anode 1 is connected

## NOTES

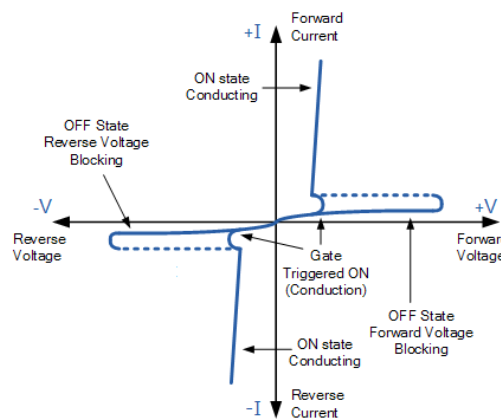
to p1, whereas anode 2 is connected to both p2 and n2. P1-n1-p2-n2 forms an SCR1 and n4-p1-n1-p2 forms SCR2. SCR1 and SCR2 are connected antiparallel to each other as shown in Figure 9.6 (b). The transistor analogy of the two antiparallel SCRs are shown in Figure 9.6 (c).



**Fig. 9.6** (a) Construction of TRIAC (b) Antiparallel SCRs as TRIAC (c) Equivalent Circuit of TRIAC

When a forward bias voltage is applied junctions J2 and J4'' are forward biased, but junction J3 is reverse biased. Junction J3 can be made to forward biased by the application of the gate pulse at p2. Similarly, when a reverse voltage is applied, the gate pulse forward biases the junction J1 and J3 making the SCR conduct in the reverse direction. In transistor analogy, during forward voltage, transistors TR2 and TR4 are ON while TR1 and TR3 are OFF. Similarly, in the reverse voltage, transistors TR1 and TR3 are ON, while TR2 and TR4 are OFF. The gate pulse may be applied to the base of the transistor TR2 in forward voltage condition and to the transistor TR3 in the reverse voltage condition to make the current conduction possible. The characteristics of TRIAC is shown in Figure 9.7.

## Characteristics of TRIAC



**Fig. 9.7** Characteristics of TRIAC

The characteristics of TRIAC is similar to the DIAC in both the first and third quadrant operation, except the presence of gate triggering in TRIAC. There exists a forward holding current ( $+I_H$ ) beyond which the forward current increases, when a forward gate pulse is applied. Similarly, there exists reverse holding current ( $-I_H$ ) beyond which the reverse current increases, when a reverse gate pulse is applied. It is to be noted that, in the first quadrant and in the third quadrant of operation, the gate pulse may either be positive or negative. Accordingly, the triggering modes in TRIAC is classified into four types.

1. I + Mode = A1 current positive (+ve), Gate current positive (+ve)
2. II – Mode = A1 current positive (+ve), Gate current negative (-ve)
3. III + Mode = A1 current negative (-ve), Gate current positive (+ve)
4. III – Mode = A1 current negative (-ve), Gate current negative (-ve)

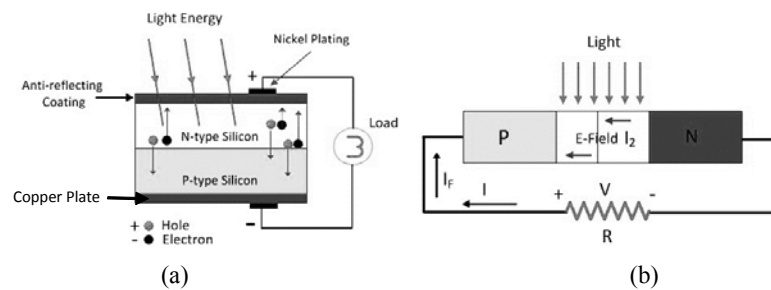
In Quadrant I, the TRIAC is usually triggered into conduction by a positive gate current, labeled above as mode I+. But it can also be triggered by a negative gate current, labeled as mode I–. Similarly, in Quadrant III, triggering with a negative gate current,  $-IG$  is also common, labeled as mode III– along with mode III+. Modes I– and III+ are, however, less sensitive configurations requiring a greater gate current to cause triggering than the more common TRIAC triggering modes of I+ and III–.

Also, just like silicon controlled rectifiers (SCR's), TRIAC's also require a minimum holding current  $I_H$  to maintain conduction at the waveforms crossover point. Then even though the two thyristors are combined into one single TRIAC device, they still exhibit individual electrical characteristics such as different breakdown voltages, holding currents and trigger voltage levels exactly the same as we would expect from a single SCR device.

## NOTES

## 9.4 SOLAR CELLS

Solar cells are the type of battery that produces a small current. They find application in all type of day to day instruments, such as solar watches, solar calculators, solar lights, solar geysers etc., the principle of working solar cell is that it converts light energy to electrical energy.



**Fig. 9.8** (a) Cross-Sectional View of Solar Cell (b) Solar Cell with a Resistive Load

## NOTES

The construction of the solar cell is given in Figure 9.8 (a). The solar cell consists of a P-type silicon semiconductor substrate above which a very thin N-type semiconductor is diffused. This combination forms a PN semiconductor diode. The N-type semiconductor is made thin because the sunlight must penetrate the N-type semiconductor must reach the depletion region ions. Above the thin N-type semiconductors, metal fingers are placed to collect the electrons from the N-type semiconductors. Solar cell does not require any external biasing voltages. An external load is connected between the metal fingers and the P-type semiconductor through the copper plate.

### 9.4.1 Working of Solar Cell

When the solar cells fall on the N-type semiconductor surface, it penetrates and reaches the depletion region formed between the P and N-type semiconductors. Depletion region consists of neutral atoms forming a barrier electric field potential. When the sun rays consisting of energy photons strike the neutral atoms in the depletion region, the electrons are knocked out of the atoms leading to holes. Hence the two charge carriers are generated inside the depletion layer. The depletion region consists of negative charges on the p side and the positive charges on the n-side constituting an electric field from N side to P side of the semiconductor as shown in Figure 9.8 (b). The knocked free electrons inside the depletion region, experiences an opposing force by the electric field present inside the depletion region. Always a force is created across a charge when it is subjected to an electric field by the following expression:

$$F = Eq$$

Where F is the force exerted on the charge, E is the electric field and q is the free charge carrier.

Now, the electrons are pushed away from the p side towards the N-type semiconductor. Similarly, the holes are pushed towards the P-type semiconductors. This leads to accumulation of the holes near the copper plate of the p side semiconductors. On the other side, the free electrons in the N-type semiconductors cannot move freely due to the property of the semiconductors but are collected by the metal fingers placed above the N-type semiconductors. The collected electrons on the metal fingers and the holes on the p side creates a large potential difference between them. When the electrical path between them is closed through a load, conventional current starts flowing from P-type to the N-type semiconductor. Thus, the solar cells do not require any external biasing but constitute to the current flow. Then the electrical path is open, each cell is designed to generate a voltage between 0.5 to 0.8V. Thus a large panel of solar cells is capable of generating large voltages. The dimensions of the metal fingers above the N-type semiconductors are such that they cover only 20% of the area of the N-type semiconductors and 80% of the remaining area is used for the sun rays to penetrate the solar cell.

The placement of the solar cells is an important factor to be considered before installing the solar panel. The sun rays consist photons with energy,  $E = hf = hc / \lambda$ . The energy of the solar rays must be larger than the band gap energy of the neutral atoms in the depletion region. A lesser photon energy will fail to dislocate the electrons in the neutral atoms and hence the energy generation will not be possible. Thus the solar cell converts the light energy to electrical energy.

## NOTES

### 9.4.2 Photodetectors

A photodetector is a device which absorbs light and converts the optical energy to measurable electric current. Detectors are classified into two types. They are:

- Thermal detectors
- Photon detectors

**Thermal Detectors:** When light falls on the device, it raises its temperature, which, in turn, changes the electrical properties of the device material, like its electrical conductivity. Examples of thermal detectors are thermopile (which is a series of thermocouples), pyroelectric detector etc.

**Photon Detectors:** Photon detectors work on the principle of conversion of photons to electrons. Unlike the thermal detectors, such detectors are based on the rate of absorption of photons rather than on the rate of energy absorption. However, a device may absorb photons only if the energy of incident photons is above a certain minimum threshold. Photon detectors, in terms of the technology, could be based on Vacuum tubes - e.g. photomultipliers or Semiconductors - e.g. photodiodes. For optical fiber applications, semiconductor devices are preferred because of their small size, good responsivity, and high speed.

### Performance Metrics of Photodetectors

There are a number of performance metrics, also called figures of merit, by which photodetectors are characterized and compared.

- **Spectral Response:** The response of a photodetector as a function of photon frequency.
- **Quantum Efficiency:** The number of carriers (electrons or holes) generated per photon.
- **Responsivity:** The output current divided by total light power falling upon the photodetector.
- **Noise-Equivalent Power:** The amount of light power needed to generate a signal comparable in size to the noise of the device.
- **Detectivity:** The square root of the detector area divided by the noise equivalent power.
- **Gain:** The output current of a photodetector divided by the current directly produced by the photons incident on the detectors, i.e., the built-in current gain.

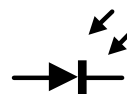


## NOTES

- **Dark Current:** The current flowing through a photodetector even in the absence of light.
- **Response Time:** The time needed for a photodetector to go from 10% to 90% of final output.
- **Noise Spectrum:** The intrinsic noise voltage or current as a function of frequency. This can be represented in the form of a noise spectral density.
- **Nonlinearity:** The RF-output is limited by the nonlinearity of the photodetector.

### Photodiodes

A photodiode is a PN junction diode that converts light energy to electric energy. Photodiodes consist of optical filters, lenses, special semiconductors that are responsive to photon energy. These photodiodes operate in the reverse biased condition, that is P-type semiconductor is supplied with a positive potential and the N-channel type semiconductor is supplied with the negative terminal. The circuit symbol of the photodiode is given in Figure 9.9. The circuit symbol is similar to the PN junction diode, but with light rays entering the diode junction.



*Fig. 9.9 Circuit Symbol of the Photodiode*

### Types of Photodiode

Photodiodes may be classified based on the construction. They are

- PN Photodiode
- Schottky Photodiode
- PIN Photodiode
- Avalanche Photodiode

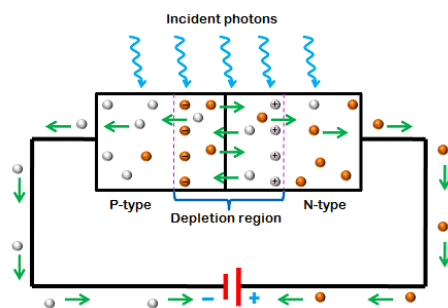
In the subsequent section, PN photodiode will be discussed.

### Construction

In the photodiode, an intrinsic layer (pure semiconductor) is inserted between the P-type and the N-type semiconductors. Such type of photodiodes is PIN photodiodes. The N-type semiconductor is a heavily doped semiconductor. A lens is placed above the depletion layer that helps the light rays to focus on it. When light rays fall on the neutral atoms, the high energy photons dislocates the electrons leaving behind free charge carriers that is electrons and the holes. The reason to insert an intrinsic semiconductor in PIN photodiodes is that, only in intrinsic semiconductors, the number of electrons is equal to holes and have a large number of electron-hole pairs forming neutral atoms. The PN junction diodes

## NOTES

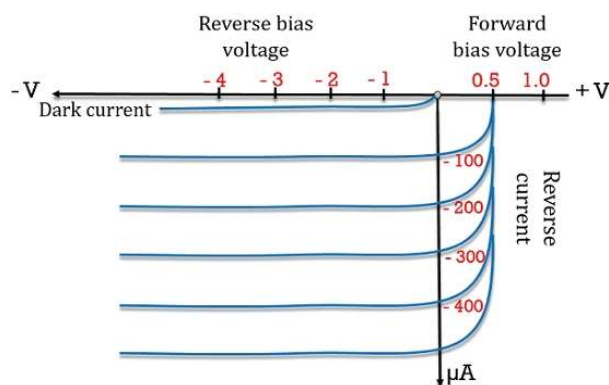
where the intrinsic semiconductors are not inserted may also work as a normal photodiode. The dislocated free charge carriers are pulled towards their respective type of semiconductors. That is, electrons are pulled towards the N side and the holes towards the P side semiconductors. The movement of these charge carriers is due to the electromotive force exerted on them by the electric field present in the depletion region.



**Fig. 9.10** Construction of the Photodiode

An external reverse bias potential is applied to the photodiode that is negative terminal is connected to the P-type and the positive terminal is connected to the N-type semiconductor. Since the electrons get injected into the n side from the depletion region, more electrons get accumulated in the n side and are attracted by the positive terminal, similarly, more holes are attracted by the negative terminal constituting the current flow from P-type to the N-type semiconductor.

Thus the light energy is converted to electrical energy. The characteristics of the photodiode are given in Figure 9.11. The characteristics are reverse biased characteristics. The dark current is the small electric current that flows through the photodiode when reverse-biased.



**Fig. 9.11** Characteristics of the Photodiode

### Applications of Photodetectors

Photodetectors are used in different applications such as radiation detection, smoke detection, flame detection and to switch on relays for street lighting.

## NOTES

The circuits that use photodiodes use either normally closed or normally open contacts depending on the desired operation.

In a *smoke detector circuit*, the photodiode is attached to a relay switch, this switch is normally closed and attached to the fire alarm. When the photodiode conducts it picks up the relay switch, this causes the normally closed switch to open preventing the alarm from activating. When the photodiode fails to conduct, the normally closed contact activates the alarm.

Photodiodes are also used in *modern oil burning furnaces* as a safety feature. The photodiode is comprised of lead sulphide and is used to detect the flame from the boiler, in the event that the flame goes out or fails to occur the photodiode opens the circuit, cutting power to the motor and step-up transformer.

Another commonly used application is *street lights*. The photodiode in the circuit uses switch-on relays to turn on the street lights when the diode fails to conduct and turns the lights off with when sufficient light is present.

Another application is the *AFM (Atomic Force Microscope)*, a laser beam is projected from a laser diode onto the back of the cantilever, and the beam is then reflected to a photodiode. The position of the beam of light on the diode gives the (x,y,z) position of the material as the probes of the cantilever scraps across the surface of the material. This gives a three-dimensional representation of the surface being scanned.

Photodiodes are also used with lasers to form a security system. When the light projected by a laser to the photodiode is broken a security alarm is tripped.

### Check Your Progress

1. What is TRIAC?
2. What are the different types of detectors?
3. Define photodiode.

## 9.5 ANSWERS TO CHECK YOUR PROGRESS

1. TRIAC is a three terminal, four layer, bidirectional semiconductor device that controls the flow of AC current and AC power in the circuit. It can conduct in both the directions.
2. Detectors are of two types i.e. thermal detectors and photon detectors.
3. A photodiode is a PN junction diode that converts light energy to electric energy. Photodiodes consist of optical filters, lenses, special semiconductors that are responsive to photon energy.

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## 9.6 SUMMARY

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- The circuit symbol of DIAC consists of two triangles connected opposite to each other with the anode terminals.
- DIAC is a five layer device consisting of N-P-N-P-N structure.
- TRIAC is a three terminal, four layer, bidirectional semiconductor device that controls the flow of AC current and AC power in the circuit. It can conduct in both the directions. In DIAC, it was necessary to drive the DIAC to breakdown voltage to make it conduct, but with the presence of gate terminal in TRIAC, the gate pulses may be applied in both the forward and reverse directions to make the TRIAC conduct.
- A photodetector is a device which absorbs light and converts the optical energy to measurable electric current.
- Photon detectors work on the principle of conversion of photons to electrons. Unlike the thermal detectors, such detectors are based on the rate of absorption of photons rather than on the rate of energy absorption.
- A photodiode is a PN junction diode that converts light energy to electric energy. Photodiodes consist of optical filters, lenses, special semiconductors that are responsive to photon energy.
- Photodetectors are used in different applications such as radiation detection, smoke detection, flame detection and to switch on relays for street lighting.

## NOTES

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## 9.7 KEY WORDS

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- **DIAC:** It is a diode that conducts electrical current only after its breakover voltage has been reached momentarily.
- **TRIAC:** It is three terminal semiconductor device that conducts current in either direction when triggered.
- **Photodetectors:** These are sensors of light having a p-n junction that converts light photons into current.

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## 9.8 SELF ASSESSMENT QUESTIONS AND EXERCISES

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### Short Answer Questions

1. Write short notes on DIAC and TRIAC
2. Draw the circuit symbol of DIAC and TRIAC.
3. Draw the equivalent structure of DIAC.

4. Differentiate DIAC and TRIAC.

### Long Answer Questions

### NOTES

1. Explain the construction and working of DIAC and TRIAC
2. What are photodetectors? Explain the performance metrics of photodetectors.
3. Write a brief description of photodetectors.
4. Explain the working of photodiodes.

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## 9.9 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

# UNIT 10 SINUSOIDAL OSCILLATORS

## NOTES

### Structure

- 10.0 Introduction
- 10.1 Objectives
- 10.2 Oscillators
  - 10.2.1 RC Phase Shift Oscillators
  - 10.2.2 Wien Bridge Oscillators
  - 10.2.3 LC Oscillators
  - 10.2.4 Colpitt's Oscillators
  - 10.2.5 Hartley Oscillators
  - 10.2.6 Crystal Oscillators
- 10.3 Answers to Check Your Progress Questions
- 10.4 Summary
- 10.5 Key Words
- 10.6 Self Assessment Questions and Exercises
- 10.7 Further Readings

## 10.0 INTRODUCTION

Having learned about transistor amplifiers, this unit focuses on the capability of transistors to generate oscillating sinusoidal voltages. Oscillators generate sinusoidal output voltage without any input provided they meet oscillation criteria called Barkhausen criteria. You will learn about various types of oscillators that include RC oscillators, RC Phase Shift oscillators, Wien Bridge oscillators, LC oscillators, Colpitt's and Hartley oscillators. The listed oscillators are designed oscillators whereas there are naturally available crystals that are used to generate such oscillating voltages. Such oscillators are called as Crystal oscillators.

## 10.1 OBJECTIVES

After going through this unit, you will be able to:

- Compare the functions of an amplifier and an oscillator
- Explain the different types of oscillator circuits
- Analyze the principle behind the working of an oscillator circuit
- Compare the different oscillator circuits and its operating ranges
- Understand the basics and the analysis of oscillator circuits, such as RC Phase shift and Wien Bridge oscillator, LC oscillators – Colpitt's and Hartley oscillator

- Learn Crystal oscillator functions and the principle behind the working of such oscillators

## NOTES

## 10.2 OSCILLATORS

Oscillators are electronic circuitry consists of passive components and transistor that are capable of generating oscillating signals without any input source. The oscillating signals are generally sinusoidal. They are different from generators by the nature of the generation of oscillating signals. Generators are capable of generating oscillating signals like sinusoidal, triangular, saw-tooth, square waveforms, whereas oscillators are limited only to sinusoidal signals.

### Working Principle

Oscillator circuits work on the principle of positive feedback. Oscillator circuit consists of an amplifier section and a feedback section. The gain of the amplifier section is considered as  $A$  and the gain of the feedback section is considered as  $\beta$ . The overall gain of the circuit for oscillators is given as

$$G_{osc} = \frac{A}{1 - A\beta}$$

### Proof:

Let the open loop gain of the amplifier be

$$A_{OL} = \frac{V_o}{V_i}$$

The gain with feedback network is given as

$$A_f = \frac{V_o}{V_s}$$

For a positive feedback,

$$V_i = V_s + V_f$$

We know that

$$V_f = \beta V_o$$

Substituting in  $V_i$  above,

$$V_i = V_s + \beta V_o$$

$$V_s = V_i - \beta V_o$$

$$A_f = \frac{V_o}{V_i - \beta V_o}$$

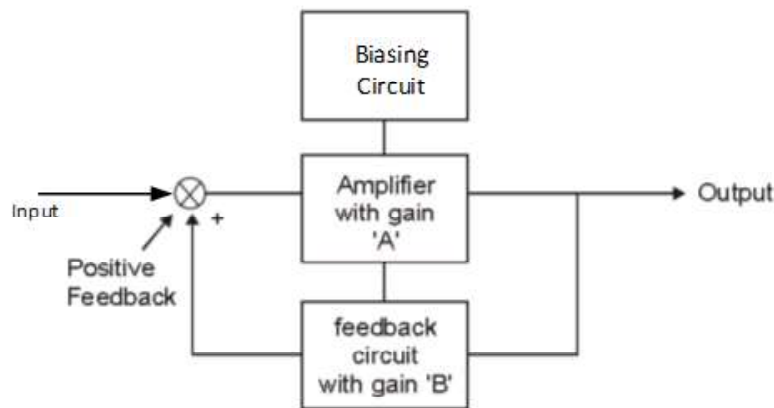
$$A_f = \frac{V_o / V_i}{1 - \beta V_o / V_i}$$

$$A_f = \frac{A}{1 - A\beta}$$

Whereas the gain of a negative feedback circuit (generally amplifiers) is given as

$$G_{amp} = \frac{A}{1 + A\beta}$$

The general block diagram of the oscillator circuit is shown in Figure 10.1.



**Fig. 10.1** Block Diagram of an Oscillator Circuit

### Condition for Oscillation

Before understanding the oscillation condition in oscillators, it is required to understand the phase shift process inside the transistor. A transistor amplifier generates a phase shift of  $180^\circ$  between its input and output. In other words, a sinusoidal input provided at the input of the transistor appears opposite on the output side of the transistor with an amplified magnitude.

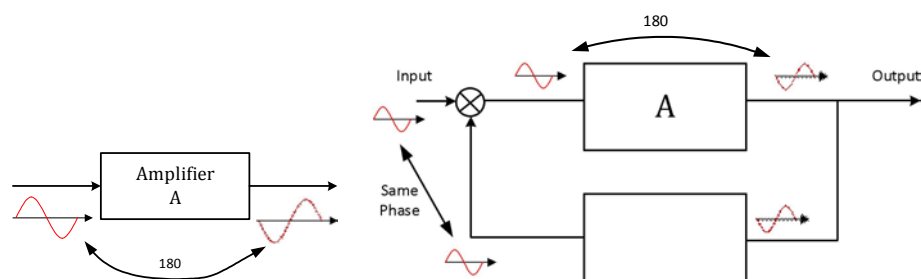
When a transistor is connected to the feedback network, the output from the feedback network that is fed to the mixer network must be in the same phase as that of the input to the amplifier. But, the input to the feedback network, which is sampled from the output of the amplifier is at a phase difference. Hence, unless the feedback network generates a phase shift of, the oscillations will never happen, since without the required phase shift, the input to the amplifier and the output of the feedback network will be out of phase with each other.

### NOTES



The Figure 10.2 shows the phase shift in an amplifier without feedback and with feedback network.

## NOTES



**Fig. 10.2** Phase Shift in Amplifier (a) Without Feedback (b) With a Feedback Network

Hence for an oscillation to start, the feedback network must generate a phase shift of  $180^\circ$ , contributing to a total of  $360^\circ$  for the total oscillator network. For a circuit to oscillate, it must satisfy Barkhausen criteria. It is given by

$$A\beta \geq 1$$

### Proof:

Consider the input voltage to the amplifier be  $V_i$  and output voltage be  $V_o$ . Therefore,

$$V_o = AV_i$$

For the feedback network,

$$V_f = \beta V_o$$

Substituting for  $V_o$  in the above equation,

$$V_f = \beta AV_i$$

The above relation relates  $V_i$  and  $V_f$ .  $V_i$  and  $V_f$  must be in the same phase and hence  $|A\beta|$  must be equal to unity. Hence the condition for oscillation, which is also known as Barkhausen criteria is given as:

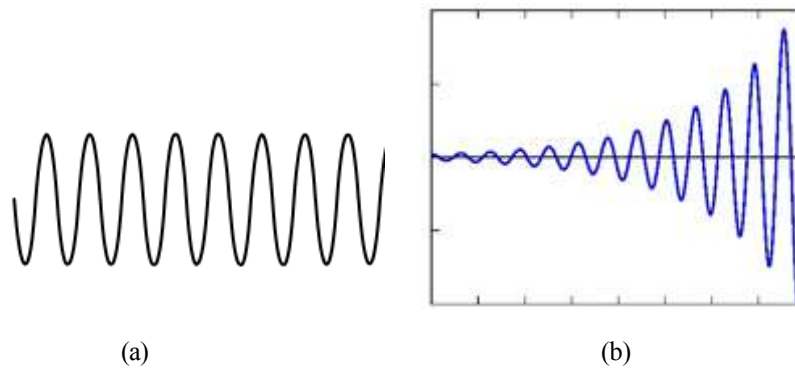
$$|A\beta| = 1$$

The condition provided above is the condition of instability. Oscillators work under the instability criteria. In other words

$$|A\beta| = 1 \text{ and } \angle A\beta = 2m\pi$$

where  $m$  is an integer.

When  $|A\beta| = 1$ , the oscillations will be a sustained oscillation as depicted in Figure 10.3 (a). When  $|A\beta| > 1$ , the oscillations will be a growing oscillations as shown in Figure 10.3 (b).



**Fig. 10.3** Condition for Oscillation (a)  $|A\beta| = 1$ , (b)  $|A\beta| > 1$

## NOTES

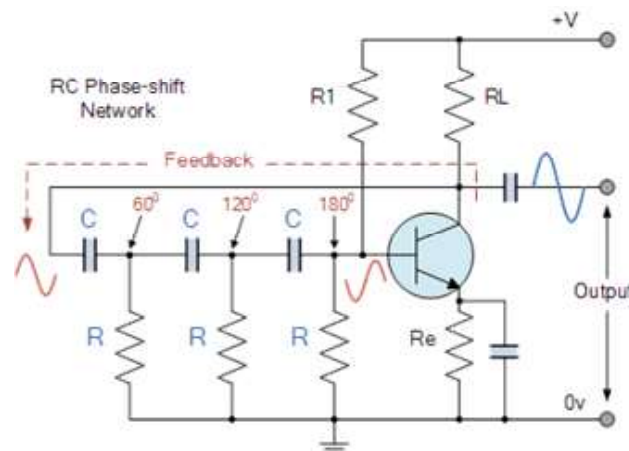
### Types of Oscillators

Following are the type of sinusoidal oscillators:

- RC Phase Shift Oscillators
- Wien Bridge Oscillators
- LC Oscillators
- Colpitt's Oscillators
- Hartley Oscillators
- Crystal Oscillators

#### 10.2.1 RC Phase Shift Oscillators

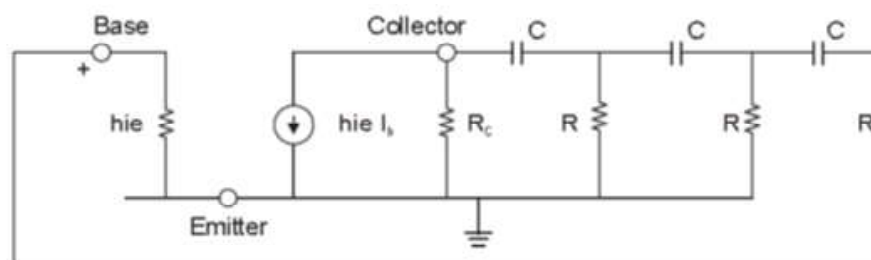
The circuit diagram of an RC phase shift oscillator is shown in Figure 10.4. The RC phase shift oscillator consists of three RC network as a feedback circuit and a biased CE amplifier circuit. For oscillations to take place there must a  $360^\circ$  of phase shift. Each RC network provides  $60^\circ$  of phase shift each, thereby producing a total of  $180^\circ$ . The amplifier circuit produces another  $180^\circ$  to produce a total of  $360^\circ$ .



**Fig. 10.4** RC Phase Shift Oscillator

## NOTES

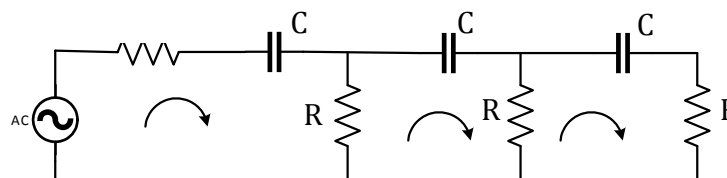
For the purpose to determine the oscillating resonant frequency, it is important to replace the amplifier circuit with its hybrid equivalent circuit. Therefore the equivalent circuit model of an RC phase shift oscillator circuit is given in Figure 10.5 after replacing all the coupling capacitors in the amplifier circuit with a short circuit.



**Fig. 10.5** Equivalent Circuit Model of RC Phase Shift Oscillator

The biasing circuit resistance  $R_1$  do not contribute to the resonant frequency and hence are neglected. Similarly, when  $C_E$  is replaced with a short circuit,  $R_E$  does not have any effect.

The equivalent circuit is further simplified for loop analysis as shown in Figure 10.6. It is presumed that  $h_{ie} + R$  (the last  $R$  connecting  $h_{re}$ ) =  $R'$ . But for the sake of simplicity, let  $R' = R$ .



**Fig. 10.6** Simplified Equivalent Circuit Model of an RC Phase Shift Oscillator Circuit

Applying KVL in all the loops,

$$I_1 R_c + I_1 (-jX_c) + R(I_1 - I_2) = -h_{fe} I_b R_c$$

$$R(I_1 - I_2) + I_2 (-jX_c) + R(I_2 - I_3) = 0$$

$$R(I_3 - I_2) + I_3 (-jX_c) + I_3 R = 0$$

Where  $X_c = \frac{1}{\omega C}$ , Rearranging

$$I_1 (R_c - jX_c + R) - I_2 R = -h_{fe} I_b R_c - I_1 R + I_2 (2R - jX_c) - I_3 R = 0$$

$$-I_2 (R) + (2R - jX_c) I_3 = 0$$

$$\begin{bmatrix} R_c - jX_c + R & -R & 0 \\ -R & 2R - jX_c & -R \\ 0 & -R & 2R - jX_c \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -h_{fe} I_b R_c \\ 0 \\ 0 \end{bmatrix}$$

$-jX_c = \frac{1}{j\omega C} = \frac{1}{sC}$  in Laplace technique (replace  $j\omega = s$ ). Therefore the matrix becomes

$$\begin{bmatrix} R_c + \frac{1}{sC} + R & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -h_{fe} I_b R_c \\ 0 \\ 0 \end{bmatrix}$$

Using Cramer's rule,  $I_3$  can be obtained as below

$$I_3 = \frac{\Delta_3}{\Delta}$$

Therefore replace the last column of the matrix by the right-hand side matrix,

$$I_3 = \frac{\begin{vmatrix} R_c + \frac{1}{sC} + R & -R & -h_{fe} I_b R_c \\ -R & 2R + \frac{1}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}}{\Delta}$$

Where  $\Delta = \begin{vmatrix} R_c + \frac{1}{sC} + R & -R & 0 \\ -R & 2R + \frac{1}{sC} & -R \\ 0 & -R & 2R + \frac{1}{sC} \end{vmatrix}$

Replacing  $s = j\omega$ ,  $s^2 = -\omega^2$  and  $s^3 = -j\omega^3$ , equating the imaginary parts to zero

$$\omega_r = \frac{1}{RC\sqrt{\frac{4R_c + 6R}{R}}} \quad f_r = \frac{1}{2\pi RC\sqrt{\frac{4R_c}{R} + 6}}$$

## NOTES

Equating the real part, we obtain the condition for the value of  $h_{fe}$ , which is given as:

$$h_{fe} > 23 + \frac{R_c}{R} \left( 4 + 29 \frac{R^2}{R_c^2} \right)$$

## NOTES

### Advantages of RC Phase Shift Oscillators

1. It uses an RC ladder network which is simple to design.
2. Produces a consistent oscillations
3. Debugging of the circuit is easy
4. The frequency range of oscillations is in the audible ranges.
5. Does not require stabilization circuits
6. Provides a frequency stability

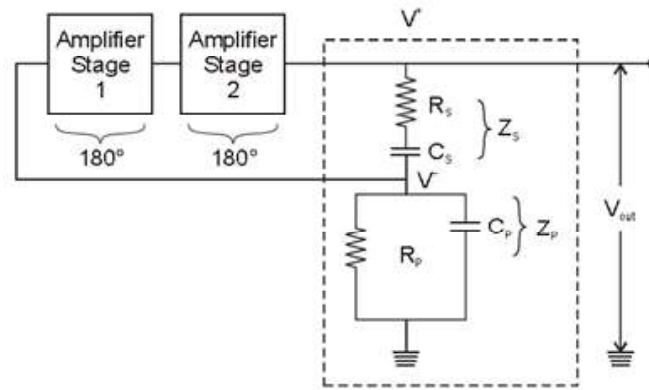
### Disadvantages of RC Phase Shift Oscillators

1. Matching the ladder network values of R and C are difficult.
2. Operates in a low-frequency range
3. Initiating oscillations are difficult.
4. Unless the RC network is matched, the stability of the oscillations cannot be sustained.

### 10.2.2 Wien Bridge Oscillators

Wien bridge oscillator consists of an amplifier module and a feedback module. The feedback circuit consists of a series RC network in series with a parallel RC network. This type of feedback network is called a lead-lag network. At low frequency, the series capacitor becomes open and the shunt capacitor becomes short and vice versa for higher frequencies. The series RC network in the feedback circuit is called as high pass filter stage and parallel RC network is called as a low pass filter stage.

Generally, the Wein bridge oscillator circuit consists of two transistor amplifier stage to generate  $360^\circ$  phase shift. The schematic diagram of a Wien bridge oscillator circuit is shown in Figure 10.7.



**Fig. 10.7** Wien Bridge Oscillator

In Figure 10.7,

$$Z_P = R_P \parallel sC_P \quad Z_S = R_S + \frac{1}{sC_S}$$

For the feedback network, the feedback gain  $\beta$  is given as

$$\beta = \frac{V^+}{V^-} = \frac{Z_P}{Z_P + Z_S} = \frac{(R_P \parallel sC_P)}{R_S + \frac{1}{sC_S} + (R_P \parallel sC_P)} = \frac{\frac{R_P}{1 + sR_P C_P}}{\frac{1 + sR_S C_S}{sC_S} + \frac{R_P}{1 + sR_P C_P}}$$

Rearranging and simplifying the above expression,

$$\beta = \frac{sR_P C_S}{s^2 R_S R_P C_S C_P + s(R_P C_P + R_S C_S + R_P C_S) + 1}$$

The overall gain of the oscillator circuit is given as  $A\beta$ , replacing  $s = j\omega, s^2 = -\omega^2$

$$A\beta = A \frac{j\omega R_P C_S}{-\omega^2 R_S R_P C_S C_P + j\omega(R_P C_P + R_S C_S + R_P C_S) + 1}$$

Therefore, equating the real part

$$1 - \omega^2 R_S R_P C_S C_P = 0 \quad \omega^2 = \frac{1}{R_S R_P C_S C_P} \quad f_r = \frac{1}{2\pi \sqrt{R_S R_P C_S C_P}}$$

Similarly, equating the imaginary part, and if  $R_S = R_P = R$  and  $C_S = C_P = C$ , then

$$A\beta = \frac{A}{3}$$

Hence, the condition for stability is  $A = 3$ .

## NOTES

**Table 10.1** Comparison of Phase Shift Oscillator and Wien Bridge Oscillator

**NOTES**

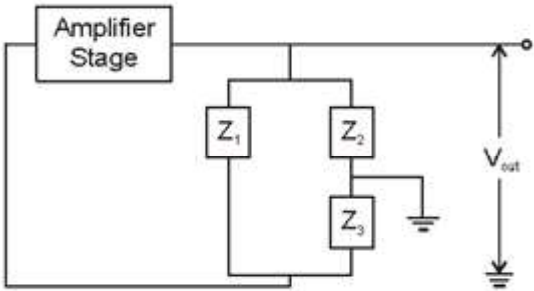
S. No	RC Phase Shift Oscillator	Wien Bridge Oscillator
1.	It consists of three RC network.	It consists of a lead-lag network
2.	The feedback network generates a phase shift of $180^\circ$ .	Feedback network does not generate any phase shift.
3.	The amplifier section generates a phase shift of $180^\circ$ .	The amplifier generates a phase shift of $360^\circ$ .
4.	The frequency of oscillation is $f_r = \frac{1}{2\pi RC \sqrt{\frac{4R_c}{R} + 6}}$	The frequency of oscillation is $f_r = \frac{1}{2\pi \sqrt{R_s R_p C_s C_p}}$
5.	The condition for stability is $h_{fe} > 23 + \frac{R_c}{R} \left( 4 + 29 \frac{R^2}{R_c^2} \right)$	The condition for stability is $A = 3$

**10.2.3 LC Oscillators**

The oscillator circuits consisting of a combination of L and C components in their feedback network are categorized as LC oscillators. Some of the LC oscillator circuits are:

- Colpitt's Oscillator
- Clapp Oscillator
- Hartley Oscillator
- Armstrong Oscillator
- Crystal Controlled Oscillators

The general structure of an LC oscillator circuit is as shown in Figure 10.8.



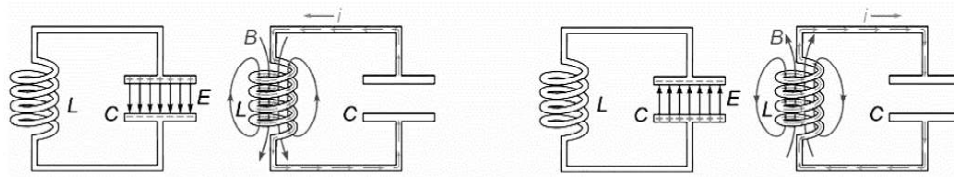
**Fig. 10.8** General LC Oscillator

The circuit consisting of L and C are generally known as a tank circuit. When L and C are connected in parallel, there will be a transfer of charges between

L and C indefinitely resulting in a tank/storage of charge. Oscillators that employ tank circuits are generally used for high-frequency oscillations. The frequency can be controlled by the values of L and C.

### Working Principle of LC Circuits

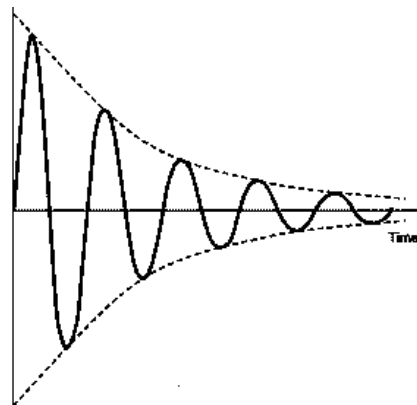
Assume that the capacitor is charged initially by a DC voltage source. In a tank circuit, the charged capacitor discharges its charges to the inductor. Inductor generates a magnetic field. This process continues until the strength of the magnetic field is greater than the charge of the capacitor. Once the magnetic field acquires enough strength, according to Lenz law, the capacitor is charged, but in the opposite direction. The charging of the capacitor continues, until the capacitor acquires strength more than the magnetic field strength. A simplified illustration of the same is given in Figure 10.9. Due to the internal losses in the capacitor and inductor, the magnitude of the charging capacitor between different cycle reduces resulting in a damped oscillation as shown in Figure 10.10.



**Fig. 10.9** Tank Circuit Illustration

The frequency of oscillation for an LC circuit is given as:

$$f = \frac{1}{2\pi\sqrt{LC}}$$



**Fig. 10.10** Damped Oscillations Across the Tank Circuit

### 10.2.4 Colpitt's Oscillators

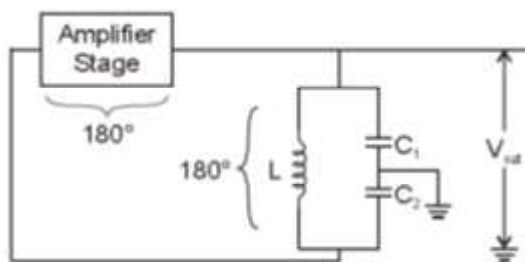
The schematic diagram of the Colpitt's oscillator is shown in Figure 10.11. Colpitt's oscillator consists of an amplifier stage and a feedback network each contributing

### NOTES



## NOTES

to  $180^\circ$  phase shift to amount to a total of  $360^\circ$  phase shift. The feedback network consists of an inductor  $L$ , and capacitors  $C_1$  and  $C_2$  connected as shown in Figure 10.11. The feedback circuit constitutes a tank circuit. On proper biasing of the amplifier circuit, initially, the capacitors charge and discharge to the inductors. Since the feedback circuit is a tank circuit charging and discharging takes place continuously resulting in a sustained oscillations.



**Fig. 10.11** Colpitt's Oscillator

In the Colpitt's oscillator, the condition for oscillation is determined when the imaginary components are equated to zero. The tank circuit consists of two capacitances resulting in capacitive reactance  $X_{C_1}$ ,  $X_{C_2}$  and an inductive reactance  $X_L$ . Therefore,

$$X_{C_1} = \frac{1}{j\omega C_1} \quad X_{C_2} = \frac{1}{j\omega C_2} \quad X_L = j\omega L \quad X_{C_1} + X_{C_2} + X_L = 0$$

$$\Rightarrow \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} + j\omega L = 0 \Rightarrow \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} = -j\omega L$$

$$\Rightarrow \frac{1}{\omega C_1} + \frac{1}{\omega C_2} = -j^2 \omega L \Rightarrow \frac{1}{\omega C_1} + \frac{1}{\omega C_2} = \omega L$$

$$\Rightarrow \frac{1}{C_1} + \frac{1}{C_2} = \omega^2 L \Rightarrow \omega^2 = \frac{1}{L} \left\{ \frac{1}{C_1} + \frac{1}{C_2} \right\}$$

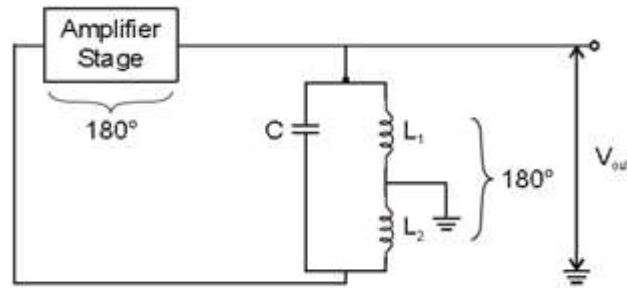
$$\omega = \frac{1}{\sqrt{L}} \sqrt{\frac{C_1 + C_2}{C_2 C_1}} \quad f_r = \frac{1}{2\pi \sqrt{L C_{eq}}}$$

where

$$C_{eq} = \frac{C_2 C_1}{C_1 + C_2}$$

### 10.2.5 Hartley Oscillators

The schematic diagram of Hartley's oscillator is shown in Figure 10.12.



**Fig. 10.12** Hartley Oscillator

The difference between Hartley's oscillator and Colpitt's oscillator are in the tank circuit, inductors are replaced with capacitors and capacitors are replaced with the inductor. The working of Hartley oscillator is also similar to that of the Colpitt's oscillator. The condition for the oscillation is also obtained similarly to the Colpitt's oscillator. In Hartley oscillator,

$$X_{L_1} = j\omega L_1 \quad X_{L_2} = j\omega L_2 \quad X_C = \frac{1}{j\omega C} \quad X_{L_1} + X_{L_2} + X_C = 0$$

$$j\omega L_1 + j\omega L_2 + \frac{1}{j\omega C} = 0 \quad j\omega L_1 + j\omega L_2 = -\frac{1}{j\omega C}$$

$$\omega L_1 + \omega L_2 = \frac{1}{\omega C}$$

$$\omega^2 = \frac{1}{C(L_1 + L_2)} \quad \omega = \frac{1}{\sqrt{C(L_1 + L_2)}} \quad f_r = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}$$

### 10.2.6 Crystal Oscillators

Crystal oscillators operate on the principle of the piezoelectric effect. When the oscillator circuits and tuned circuits are replaced with crystals instead of tank circuits, they form a crystal oscillator.

Crystal oscillators are preferred when stable oscillations are required over longer periods. Usually, quartz crystal is used as a resonant circuit for consistent oscillations that replaces the tank circuit.

When a solid structure is subjected to mechanical stress, the solid structure experiences potential or oscillations across the opposite faces of the crystal that are used as resonator circuits. This property of a crystal is called **piezoelectric effect**. The equivalent circuit of quartz crystal is given below in Figure 10.13.

## NOTES

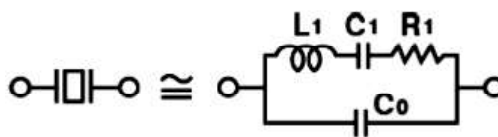


Fig. 10.13 Crystal Oscillator

## NOTES

**Description**

- These crystals have a quality factor,  $Q$  ranging more than 20,000.
- In crystal oscillators, two resonant conditions occur
  - (i) Series resonance: It occurs across  $R_1$ ,  $L_1$ , and  $C_1$ . For series resonance,  $R_1$  is very low.
  - (ii) Parallel resonance or anti-resonance: It occurs when the series resonance is equal to the capacitive reactance of  $C_0$ . For anti-resonance  $R_1$  is very high.
- The series RLC portion is referred to as the *motional arm* of the circuit and arises from the mechanical crystal vibrations.
- The  $R_1$  represents the heat losses due to mechanical friction in the crystal.
- The inductor  $L_1$  is the electrical equivalent of the crystal mass and the capacitor  $C_1$  represents the crystal elasticity.
- $C_0$  is called the static capacitance – it is the capacitance associated with the crystal and its adherent electrodes plus the stray capacitance internal to the crystal enclosure.

**Derivation for Crystal Oscillator**

For the equivalent circuit shown in Figure 10.13. Let

$$Z_0 = \frac{1}{j\omega C_0} \quad Z_1 = R_1 + j\omega L_1 + \frac{1}{j\omega C_1}$$

Equivalent impedance  $Z_{eq}$  is given as

$$\begin{aligned}
 Z_{eq} &= \frac{Z_1 Z_0}{Z_1 + Z_0} = \frac{\left( R_1 + j\omega L_1 + \frac{1}{j\omega C_1} \right) \frac{1}{j\omega C_0}}{R_1 + j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_0}} \\
 &= \frac{\frac{\omega L_1 - \frac{1}{\omega C_1}}{\omega C_0} - j \frac{R_1}{\omega C_0}}{R_1 + j \left( \omega L_1 - \frac{1}{\omega C_1} - \frac{1}{\omega C_0} \right)}
 \end{aligned}$$

$$= \frac{a + jb}{c + jd} \times \frac{c - jd}{c - jd} = \frac{ac + bd + j(bc - ad)}{c^2 + d^2}$$

$$= \frac{ac + bd}{c^2 + d^2} + j \frac{bc - ad}{c^2 + d^2} = R_{eq} + jX_{eq}$$

For resonance, the imaginary term must be equal to zero, or in other words the  $Z_{eq}$  must be purely resistive and therefore,

$$X_{eq} = \frac{bc - ad}{c^2 + d^2} = 0 \Rightarrow bc - ad = 0 \Rightarrow bc = ad$$

$$\frac{-R_1^2}{\omega_r C_0} = \left( \frac{\omega_r L_1 - \frac{1}{\omega_r C_1}}{\omega_r C_0} \right) \left( \omega_r L_1 - \frac{1}{\omega_r C_1} - \frac{1}{\omega_r C_0} \right)$$

$$-R_1^2 = \left( \omega_r L_1 - \frac{1}{\omega_r C_1} \right) \left( \omega_r L_1 - \frac{1}{\omega_r C_1} - \frac{1}{\omega_r C_0} \right)$$

$$\omega_r^2 L_1^2 - \frac{L_1}{C_1} - \frac{L_1}{C_0} - \frac{L_1}{C_1} + \frac{1}{\omega_r^2 C_1^2} + \frac{1}{\omega_r^2 C_1 C_0} + R_1^2 = 0$$

$$\omega_r^4 + \left( \frac{R_1^2}{L_1^2} - \frac{2}{L_1 C_1} - \frac{1}{L_1 C_0} \right) \omega_r^2 + \frac{1}{L_1^2 C_1^2} + \frac{1}{L_1^2 C_1 C_0} = 0$$

Solving the quadratics equation for  $\omega_r^2$ ,

$$\omega_r^2 = \frac{1}{2} \left\{ \left( \frac{2}{L_1 C_1} + \frac{1}{L_1 C_0} - \frac{R_1^2}{L_1^2} \right) \pm \left[ \left( \frac{2}{L_1 C_1} + \frac{1}{L_1 C_0} - \frac{R_1^2}{L_1^2} \right)^2 - 4 \left( \frac{1}{L_1^2 C_1^2} + \frac{1}{L_1^2 C_1 C_0} \right) \right]^{1/2} \right\}$$

Pulling out 4 from the square root term

$$\begin{aligned} & \left[ \left( \frac{1}{L_1 C_1} + \frac{1}{2L_1 C_0} - \frac{R_1^2}{2L_1^2} \right)^2 - \left( \frac{1}{L_1^2 C_1^2} + \frac{1}{L_1^2 C_1 C_0} \right) \right]^{1/2} \\ &= \left[ \frac{1}{L_1^2 C_1^2} + \frac{1}{L_1^2 C_1 C_0} - \frac{R_1^2}{L_1^3 C_1^2} + \frac{1}{4L_1^2 C_0} - \frac{R_1^2}{2L_1^3 C_1 C_0} + \frac{R_1^4}{4L_1^4} - \frac{1}{L_1^2 C_1^2} - \frac{1}{L_1^2 C_1 C_0} \right]^{1/2} \\ &= \left[ \left( \frac{1}{2L_1 C_0} - \frac{R_1^2}{2L_1^2} \right) - \frac{R_1^2}{L_1^3 C_1} \right]^{1/2} \end{aligned}$$

## NOTES

**NOTES**

Substituting the above equation in the resonance condition equation,

$$\omega_r^2 = \frac{1}{2} \left\{ \left( \frac{2}{L_1 C_1} + \frac{1}{L_1 C_0} - \frac{R_1^2}{L_1^2} \right) \pm \left[ \left( \frac{1}{2L_1 C_0} - \frac{R_1^2}{2L_1^2} \right) - \frac{R_1^2}{L_1^3 C_1} \right]^{1/2} \right\}$$

Generally,

$$\frac{1}{2L_1 C_0} - \frac{R_1^2}{2L_1^2} \gg \frac{R_1^2}{L_1^3 C_1}$$

Hence  $\frac{R_1^2}{L_1^3 C_1}$  can be neglected. Therefore the resonance condition expression may be approximated as

$$\omega_r^2 \approx \frac{1}{2} \left\{ \left( \frac{2}{L_1 C_1} + \frac{1}{L_1 C_0} - \frac{R_1^2}{L_1^2} \right) \pm \left[ \left( \frac{1}{2L_1 C_0} - \frac{R_1^2}{2L_1^2} \right) \right]^{1/2} \right\}$$

Observing the above equation, there are two possibilities of the resonant condition, one for + sign and other for the – sign.

For the + sign,  $\omega_r^2$  reduces to

$$\omega_{rs} \approx \frac{1}{\sqrt{L_1 C_1}}$$

The above condition is called the SERIES RESONANCE condition. Similarly for – sign,

$$\omega_{rp} \approx \sqrt{\frac{1}{L_1 C_1} + \frac{1}{L_1 C_0} - \frac{R_1^2}{L_1^2}} \quad \text{Further, the expression may be simplified as}$$

$$\frac{1}{L_1 C_0} \gg \frac{R_1^2}{L_1^2} \quad \text{Therefore neglecting } \frac{R_1^2}{L_1^2},$$

$$\omega_{rp} \approx \sqrt{\frac{1}{L_1 (C_1 + C_0)}}$$

The above condition is called the PARALLEL RESONANCE condition.

**Important Formula:**

$$G_{osc} = \frac{A}{1 - A\beta}$$

$$G_{amp} = \frac{A}{1 + A\beta}$$

- The condition for oscillation is  $A\beta \geq 1$
- RC phase shift oscillators

$$f_r = \frac{1}{2\pi RC \sqrt{\frac{4R_c}{R} + 6}}$$

$$h_{fe} > 23 + \frac{R_c}{R} \left( 4 + 29 \frac{R^2}{R_c^2} \right)$$

- Wien bridge oscillator

$$f_r = \frac{1}{2\pi \sqrt{R_s R_p C_s C_p}}$$

- The frequency of oscillation for an LC circuit

$$f = \frac{1}{2\pi \sqrt{LC}}$$

- Colpitt's oscillator

$$f_r = \frac{1}{2\pi \sqrt{LC_{eq}}}$$

Where

$$C_{eq} = \frac{C_2 C_1}{C_1 + C_2}$$

- Hartley oscillator

$$f_r = \frac{1}{2\pi \sqrt{C(L_1 + L_2)}}$$

- Crystal oscillators

**Series Resonance Condition:**  $\omega_{rs} \approx \frac{1}{\sqrt{L_1 C_1}}$

**Parallel Resonance:**  $\omega_{rp} \approx \sqrt{\frac{1}{L_1 (C_1 + C_0)}}$

## NOTES

**NOTES****Check Your Progress**

1. What is an oscillator?
2. State the Barkhausen criterion for oscillation.
3. Name two high-frequency oscillators.
4. Define piezoelectric effect.

**10.3 ANSWERS TO CHECK YOUR PROGRESS**

1. An oscillator is an electronic device, which produces an output signal of any desired frequency without any input signal.
2. The two important and necessary conditions are
  - (i) The feedback must be positive.
  - (ii) Feedback factor must be unity i.e.  $|A\beta| = 1$ .
3. Two types of high frequency oscillator are:
  - (i) Hartley Oscillator
  - (ii) Colpitt's Oscillator
4. When a solid structure is subjected to mechanical stress, the solid structure experiences potential or oscillations across the opposite faces of the crystal that are used as resonator circuits. This property of a crystal is called piezoelectric effect.

**10.4 SUMMARY**

- Oscillators work on the positive feedback principle.
- Oscillators do not have any input.
- The barkhausen criterion for oscillations include  $|A\beta| = 1$ .
- The overall loop gain of the oscillator circuit must be greater than unity for sustained oscillations to take place.
- In RC phase shift oscillator the frequency of oscillation is

$$f_r = \frac{1}{2\pi RC \sqrt{\frac{4R_c}{R} + 6}}$$

- In RC phase shift oscillator the condition for stability is

$$h_{fe} > 23 + \frac{R_c}{R} \left( 4 + 29 \frac{R^2}{R_c^2} \right)$$

- Each RC network in RC phase shift oscillator generates a  $60^\circ$  phase shift.
- Total phase shift generated by the RC feedback network is  $180^\circ$ .
- The amplifier section of the RC phase shift oscillator generates a  $180^\circ$  phase shift.
- In Wien bridge oscillator, the feedback network does not generate any phase shift.
- In Wien bridge oscillator, the condition for stability is  $A = 3$ .
- In Wien bridge oscillator, the frequency of oscillation is

$$f_r = \frac{1}{2\pi\sqrt{R_S R_P C_S C_P}}$$

- In Wien bridge oscillator, The amplifier generates a phase shift of  $360^\circ$ .
- Some of the LC oscillators will include Colpitt's Oscillator, Clapp oscillator, Hartley oscillator, Armstrong oscillator, and crystal controlled oscillators.
- The feedback network in Colpitt's oscillator consists of an inductor  $L$  connected in parallel with series connected capacitors  $C_1$  and  $C_2$ .
- The frequency of oscillation in the Colpitts oscillator is

$$f_r = \frac{1}{2\pi\sqrt{L\left\{\frac{C_2 C_1}{C_1 + C_2}\right\}}}$$

- The feedback network in Hartley's oscillator consists of a capacitor  $C$  connected in parallel with series connected inductors  $L_1$  and  $L_2$ .

- The frequency of oscillation in Hartley's oscillator,  $f_r = \frac{1}{2\pi\sqrt{C(L_1 + L_2)}}$

- Crystal oscillators work under the principle of the piezoelectric effect.
- Crystal oscillators generate both series and parallel resonance.
- Crystal oscillators are tuned circuit oscillators
- Crystal oscillators do not require maintenance and are stable oscillators over a longer period of time.
- The Q factor of the crystal is very high.

## NOTES



## NOTES

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**10.5 KEY WORDS**


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- **Oscillator:** It is an electronic device, which produces an output signal of any desired frequency without any input signal.
  - **Impedance:** It is the effective resistance of an electric component to alternating current, arising as the combined effects of ohmic resistance and reactance.
  - **Piezoelectric effect:** It is the ability of certain materials to generate an electric charge on applying mechanical stress.
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**10.6 SELF ASSESSMENT QUESTIONS AND EXERCISES**


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**Short Answer Questions**

1. Write a short note on oscillator.
2. How can an oscillator be considered as an amplifier?
3. What are the different types of oscillator circuits?
4. How does RC phase shift oscillator generate 360° cycle of phase shift?
5. Compare the resonant frequency expressions for RC Phase Shift oscillator, Wein bridge oscillator, Colpitts oscillator, and Hartley's oscillator.
6. What are the advantages of crystal oscillator?

**Long Answer Questions**

1. Explain about Colpitt's oscillator and derive the expression for the frequency of oscillation and condition of oscillation.
2. Explain about Hartley oscillator and derive the expression for the frequency of oscillation and condition of oscillation.
3. Explain the operation of the crystal oscillator with a neat diagram and write the expression for its frequency of oscillation.
4. A Colpitt's oscillator is designed with  $C_1 = 100\text{pf}$  and  $C_2 = 7500\text{pf}$ . The inductance is variable. Determine the range of inductance values, if the frequency of oscillation is to vary between 950 KHz and 2050 KHz.
5. Describe the working of a Wien bridge oscillator. Derive an expression for the resonant frequency. Give its advantages and disadvantages?
6. Explain the operation of an RC phase shift oscillator and derive the condition for oscillation and the resonant frequency with BJT.

7. A Hartley oscillator is designed with  $L_1 = 2\text{mH}$ ,  $L_2 = 20\mu\text{H}$ , and a variable capacitance. Determine the range of capacitance value if the frequency of oscillation is varied between 950 to 2050 kHz.

*Sinusoidal Oscillators*

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## 10.7 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

## NOTES

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**BLOCK - IV**  
**OPERATIONAL AMPLIFIER**

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**NOTES**

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**UNIT 11 INTRODUCTION TO  
OP-AMP**

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**Structure**

- 11.0 Introduction
- 11.1 Objectives
- 11.2 OP-AMP
  - 11.2.1 Stages of OP-AMP
  - 11.2.2 Working of OP-AMP
  - 11.2.3 The Equivalent Circuit of OP-AMP
- 11.3 Answers to Check Your Progress
- 11.4 Summary
- 11.5 Key Words
- 11.6 Self Assessment Questions and Exercises
- 11.7 Further Readings

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**11.0 INTRODUCTION**

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In this unit, you will learn about the operational amplifiers. An operational amplifier is very high-gain differential amplifier with high-input impedance and low-output impedance. The amplifiers discussed earlier can be used for certain applications like arithmetic operations, signal generations, etc., OP-AMPs are available in IC form. Since OP-AMPs are available in ICs they have become cost-effective, easy to use, less power consuming, cheaper and small size. The cost of such ICs is also considerably much cheaper making them most relevant device in today's electronics world. OP-AMPs got their name as operational amplifiers for their extensive application as arithmetic operators.

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**11.1 OBJECTIVES**

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After going through this unit, you will be able to:

- Explain the operational amplifier and its pin diagram
- Understand the various stages of OP-AMP
- Explain the working of OP-AMP
- Discuss the advantages of negative feedback circuit

## 11.2 OP-AMP

OP-AMP is available in an IC form. The most popular OP-AMP is IC 741. It consists of 8 pins packed in a Dual in-line (DIP) package. OP-AMP is represented in the form of a triangle as shown in Figure 11.1. The IC of the OP-AMP consists of the following pins:

- Pin 1: Offset Null.
- Pin 2: Inverting Input Terminal.
- Pin 3: Non-Inverting Input Terminal.
- Pin 4:  $-V_{CC}$  (Negative Voltage Supply).
- Pin 5: Offset Null.
- Pin 6: Output Voltage.
- Pin 7:  $+V_{CC}$  (Positive Voltage Supply).
- Pin 8: No Connection.

**Pin 1 and 5 – Offset Null:** OP-AMPs are very sensitive devices such that, the internal noises and disturbances may lead to the generation of the output signals. In order to overcome such unwanted signals, these pins are used to offset the voltages. Also, since OP-AMP is a high gain device, even the slightest difference between the input voltages are amplified to very large value and hence to nullify this effect, offset external voltages may be applied to these terminals of the OP-AMP.

**Pin 2 and 3:** the input voltage is applied to pins 2 and 3. Pin 2 is known as inverting input and pin 3 is known as non-inverting input. When a Voltage is applied at pin 2, the output voltage is a negative of the input voltage. Hence, the pin 2 is known as an inverting input terminal. When a voltage is applied to pin 3, the output voltage is a non-inverted output voltage.

**Pin 6:** output voltage is seen across the pin 6.

**Pin 7 and Pin 4:** The positive  $+V_{CC}$  the bias voltage is applied to pin 7 and the negative bias voltage  $-V_{DD}$  is applied across pin 4. These voltages are the saturated voltages beyond which the OP-AMP will not produce the output voltage.

**Pin 8:** no connection is made to Pin 8 and it's an open terminal.

The circuit symbol is a triangular symbol representing only the terminals as shown in Figure 11.1 (b).

### NOTES

## NOTES

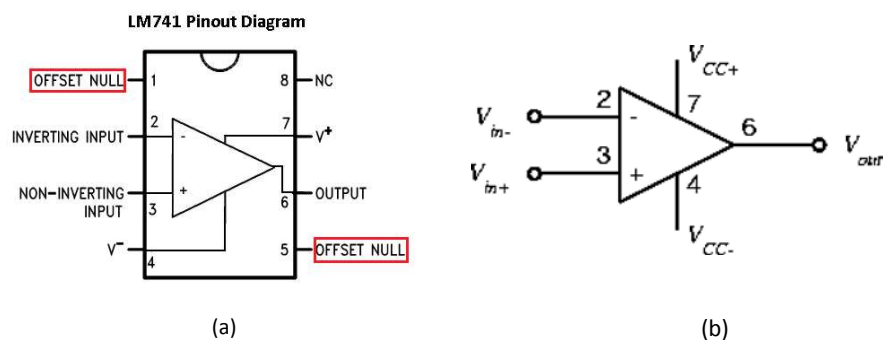


Fig. 11.1 (a) IC 741 Pin Diagram (b) Circuit Symbol of IC 741 OP-AMP

### 11.2.1 Stages of OP-AMP

The OP-AMP consists of a large number of transistors internally. There are different stages of transistors inside OP-AMP. They are an input differential amplifier stage, intermediate stage, level shifter, and the output stage.

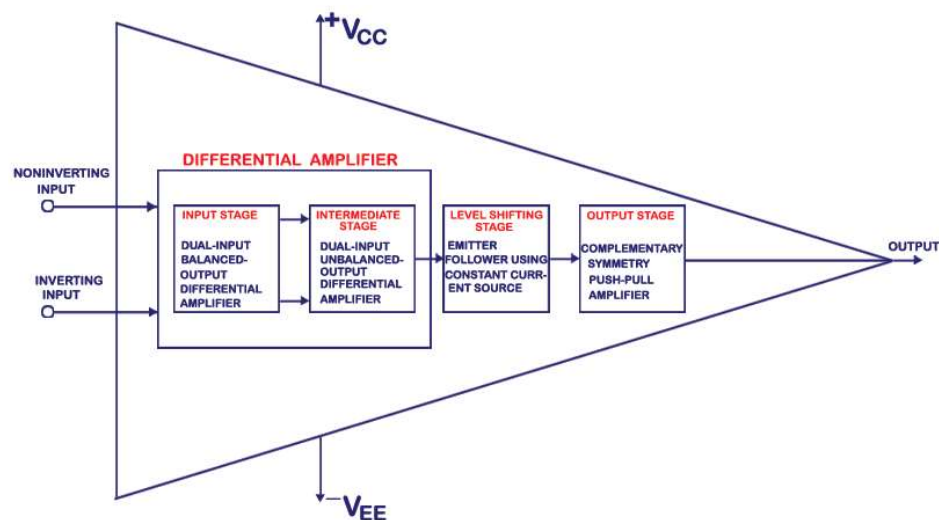


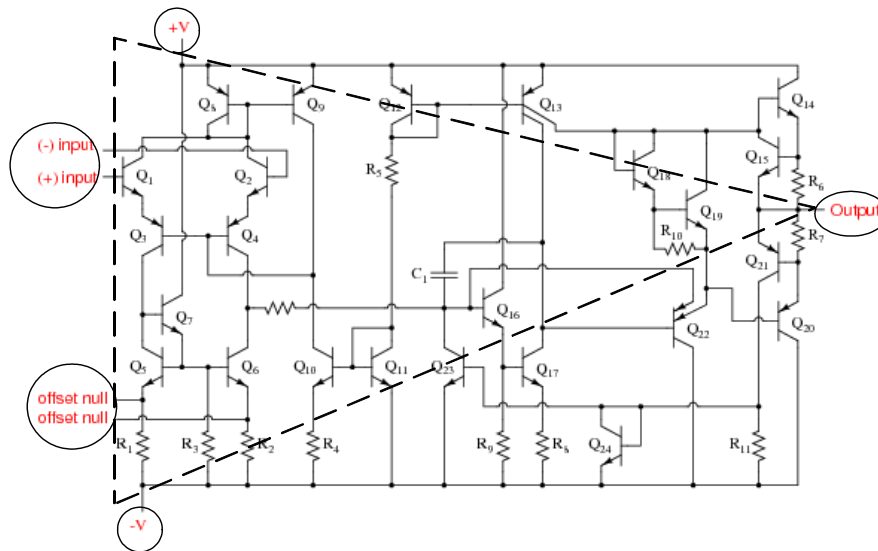
Fig. 11.2 Stages of OP-AMP

The input stage and the intermediate stage consists of differential amplifiers with very high input impedance. For an ideal OP-AMP, the input impedance the OP-AMP is considered to infinite. The input stage consists of a dual-input balanced output differential amplifier, whereas the intermediate stage consists of the dual-input unbalance output differential amplifier.

The level shifting stage consists of an emitter follower circuit inverting the form of a current source. The current source circuit drives the next stage complimentary push-pull amplifier stage. The output stage consisting of push-pull stage consists of very less output impedance. Ideally, the output impedance of the OP-AMP is zero.

Figure 11.3 shows the internal circuitry of OP-AMP. The internal circuitry of OP-AMP is complex to analyze at the transistor level and hence the OP-AMP is analyzed at the block level. The scope of this text will be to analyze the OP-AMP only using the circuit symbol. From the Figure 11.3, differential amplifiers, emitter follower circuits, biasing voltages, input, output terminals, and the push-pull amplifier terminals are clearly indicated. The biasing voltages are represented as  $+V$  and  $-V$ .

## NOTES



**Fig. 11.3** Internal Circuitry of OP-AMP

### Characteristics of Ideal OP-AMP

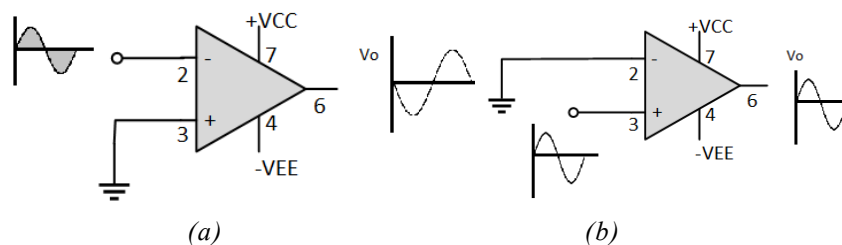
Following are the ideal characteristics of an OP-AMP.

- The input impedance of the OP-AMP is infinity,  $Z_{in} = \infty$ .
- The output impedance of the OP-AMP is zero,  $Z_{out} = 0$ .
- The open loop gain of the OP-AMP is infinity,  $A_{ol} = \infty$ .
- Operating bandwidth of OP-AMP is infinity,  $BW = \infty$ .
- Input offset voltage is zero.
- Common mode rejection ratio is infinite.
- Noise inverting OP-AMP is zero.
- Maximum output voltage range or voltage swing.
- Power supply rejection ratio is infinite.

### 11.2.2 Working of OP-AMP

Figure 11.4 shows the block diagram to explain the working of the OP-AMP.

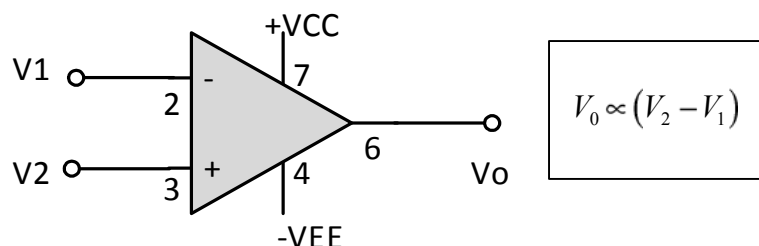
## NOTES



**Fig. 11.4** (a) Inverting Amplifier (b) Non Inverting Amplifier

When a sinusoidal input is given to the inverting terminal of the OP-AMP, and the non-inverting terminal is grounded, the output of the amplifier will have a phase shift of  $180^\circ$  and will be amplified as shown in Figure 11.4 (a). Similarly, when a sinusoidal input is fed to non-inverting terminal and the inverting terminal is grounded, the output of the OP-AMP is only amplified without any phase shift as shown in Figure 11.4 (b).

When two different voltages are given to both the inverting and non-inverting terminals of the OP-AMP, the output voltage is proportional to the difference of both the input voltages as shown inverting Figure 11.5. The voltage  $V_2$  is applied to positive terminal and voltage  $V_1$  is applied to the negative terminal, and hence the output voltage is proportional to  $V_2 - V_1$ .



**Fig. 11.5** Difference Amplifier

The proportionality in the above expression for difference amplifier may be removed by replacing the open loop differential amplifier gain. Thus, the output voltage is given as:

$$V_0 = A_{ol} (V_2 - V_1) \quad (11.1)$$

Where,  $A_{ol}$  = Open loop gain of the difference amplifier.

### Common Mode Gain

OP-AMPs in addition to the open loop differential gain,  $A_{ol}$  also, have a common mode gain,  $A_{cm}$ . Practical OP-AMPs, take into account not only the difference input voltage,  $(V_2 - V_1)$ , but also is dependent on the average of both the input voltages,  $(V_2 + V_1)/2$ . Also when both the input voltages are identical, such that, when  $V_1 = V_2$ , then the difference voltage,  $V_d = 0$  and therefore output voltage is

zero. However, practically, the output voltage is not zero even when both the input voltages are identical. The result in this mismatch is due to the presence of the common mode gain. Normally, the common mode gain is practically small compared to the differential gain and hence can be ignored.

From equation 11.1,

$$A_{ol} = \frac{V_0}{(V_2 - V_1)} = \frac{V_0}{V_d}$$

$$V_0 = A_{ol} V_d$$

Similarly,

$$A_{cm} = \frac{V_0}{V_{av}}$$

$$V_0 = A_{cm} V_{av}$$

Where,

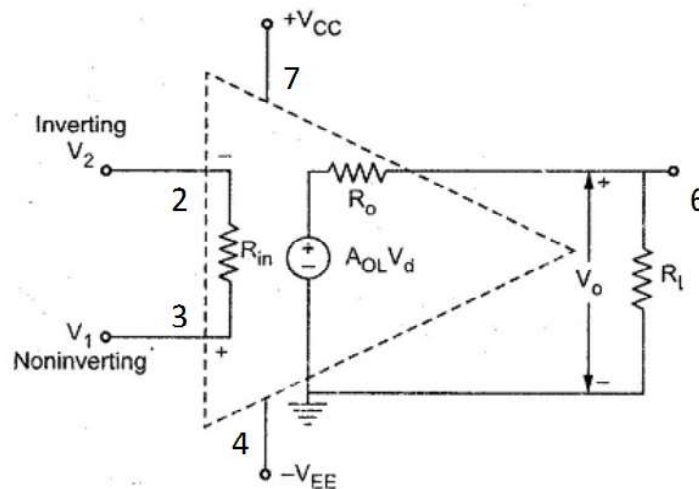
$$V_{av} = \frac{V_1 + V_2}{2}$$

In general, the output voltage is dependent on both the open loop difference gain and the common mode gain of the amplifier. Therefore,

$$V_0 = A_{ol} V_d + A_{cm} V_{av}$$

### 11.2.3 The Equivalent Circuit of OP-AMP

The ideal circuit characteristics of OP-AMP when redrawn using circuit parameters, the circuit as shown in Figure 11.6 represents the equivalent circuit of OP-AMP.



**Fig. 11.6** Equivalent Circuit of OP-AMP

## NOTES



## NOTES

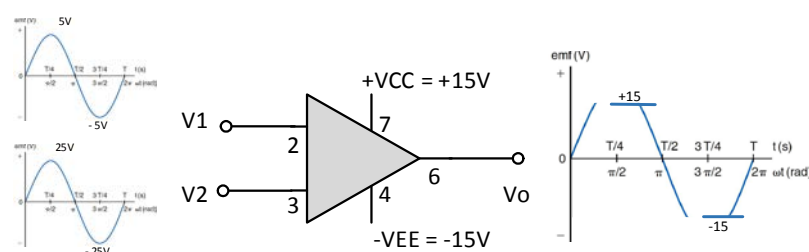
The terminal 2 and 3 corresponding to the inverting and non-inverting terminal of OP-AMP is connected to  $R_{in}$ .  $R_{in}$  is the input impedance. The input impedance of an ideal OP-AMP is infinity and hence  $R_{in} \equiv \infty$ . On the output side, the terminal 6 is connected to the load resistor  $R_p$  which is in series with the resistance  $R_o$  and a voltage source with a value equivalent to  $A_{ol}V_d$ . The resistance  $R_o$  is the output resistance of OP-AMP. The output impedance of an ideal OP-AMP is zero and hence  $R_o \equiv 0$ . That is,  $R_o$  is approximately shorted with the output terminal, such that,  $V_o = A_{ol}V_d$ , where  $V_d = V_1 - V_2$  and  $A_{ol}$  is the open loop gain of the OP-AMP.

Finally,

$$V_o = A_{ol}(V_2 - V_1) = A_{ol}V_d$$

The output side of the equivalent circuit forms a Thevenin's equivalent circuit with  $A_{ol}V_d$  equivalent to the Thevenin's voltage and  $R_o$  is equivalent to the Thevenin equivalent resistance.

### Effect of Bias Voltage on OP-AMP and Open Loop Configuration

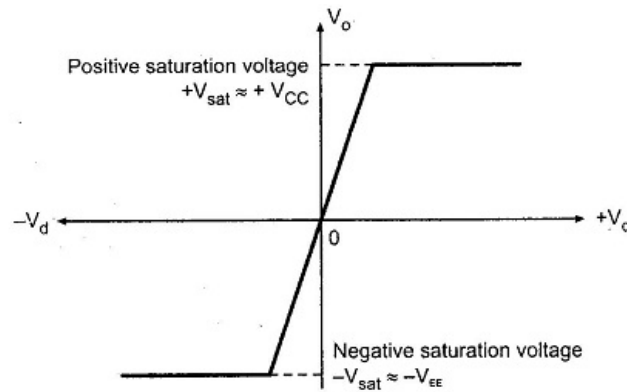


**Fig. 11.7** Effect of Bias Voltage on OP-AMP

Consider the diagram shown in Figure 11.7. The differential amplifier is fed with two input voltages  $V_1$  and  $V_2$ . Voltage  $V_1$  is sinusoidal with a maximum peak of 5 V and the voltage  $V_2$  is sinusoidal with a maximum peak of 25 V. The output voltage,  $V_o = A_{ol}(V_2 - V_1)$ . Assuming a unity gain amplifier, that is if  $A_{ol} = 1$ , then  $V_o = (25 - 5)V = 20V$ . The output voltage peak must be a sinusoidal voltage with a maximum peak of  $+20V$ . But, the output voltage in such cases, will be as shown in Figure 11.7. The output voltage will be clipped/saturated at the voltage equivalent to the bias saturation voltage of  $+V_{CC}$  and  $-V_{EE}$ . In this example, the bias saturation voltage is equal to  $\pm 15V$ . Recall, the discussion in module 2 for class B amplifiers, that, when the transistor is driven to saturation mode, the output voltage is also clipped to the saturation voltage. Also, the output voltage transfer

characteristics as shown in Figure 11.8, indicates the very small operating region of the OP-AMP between the saturation limits. The saturation voltage limits are  $+V_{CC}$  and  $-V_{EE}$ . The OP-AMP works as an amplifier only in the limited range of linear voltage between  $+V_{CC}$  and  $-V_{EE}$ . This is due to the open loop configuration of OP-AMP. Hence, the open loop configuration is not used for practical applications and closed loop configuration is preferred.

## NOTES



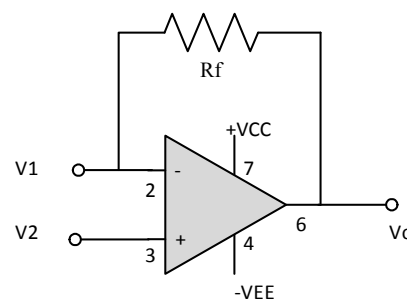
**Fig. 11.8** Transfer Characteristics of OP-AMP

### Closed Loop Negative Feedback OP-AMP

The OP-AMP circuit so far discussed contains no feedback circuit, leading to a very narrow range of operation for the amplifier. This leads to instability in the OP-AMP characteristics. This issue of instability can be avoided by providing feedback from the output to the input terminal. Feedback may be of two types:

- Positive Feedback
- Negative Feedback

Positive feedback circuits are unstable circuits that add error and the already existing error. Hence negative feedback circuits are preferred. The negative feedback circuit provides stability to the circuit and corrects the error signal. A simple closed loop OP-AMP that provides the negative feedback circuit is given in Figure 11.9.



**Fig. 11.9** Negative Feedback Circuit of OP-AMP

**NOTES**

The negative feedback circuit consists of the feedback resistor,  $R_f$  connected between the output terminal, pin 6 and the inverting input terminal, pin 2. Since the feedback resistor is connected to the negative input terminal, the feedback constitutes a negative feedback. The negative feedback resistor does not drive the transistor to saturation voltages. The gain experienced by the closed loop negative feedback OP-AMP circuit is known as closed loop gain,  $A_{cl}$  of OP-AMP. Closed loop gain is always less than the open loop gain. This reduction in the gain is due to the feedback resistor and hence the transistor is not driven to the saturation voltages.

**Advantages of Negative Feedback Circuit**

Following are the advantages of negative feedback compared to an open loop system:

- The negative feedback reduces noise.
- It has highly stabilized gain.
- It has less harmonic, amplitude and phase distortion.
- Input and output impedances can be modified as desired.
- It can increase or decrease output impedances.
- It has a higher region of linear operation.
- The circuit is more stable

**Check Your Progress**

1. What are the different stages of OP-AMP?
2. Why negative feedback circuit are preferred over positive feedback?

**11.3 ANSWERS TO CHECK YOUR PROGRESS**

1. Various stages of OP-AMP are input differential amplifier stage, intermediate stage, level shifter, and the output stage.
2. Positive feedback circuits are unstable circuits that add error and the already existing error. Hence negative feedback circuits are preferred. The negative feedback circuit provides stability to the circuit and corrects the error signal.

**11.4 SUMMARY**

- The most popular OP-AMP is IC 741. It consists of 8 pins packed in a Dual In-Line (DIP) package.

- The OP-AMP consists of a large number of transistors internally. There are different stages of transistors inside OP-AMP. They are an input differential amplifier stage, intermediate stage, level shifter, and the output stage.
- The input stage and the intermediate stage consists of differential amplifiers with very high input impedance. The input stage consists of a dual-input balanced output differential amplifier, whereas the intermediate stage consists of the dual-input unbalance output differential amplifier.
- The level shifting stage consists of an emitter follower circuit inverting the form of a current source.
- The output stage consisting of push-pull stage consists of very less output impedance.
- When a sinusoidal input is given to the inverting terminal of the OP-AMP, and the non-inverting terminal is grounded, the output of the amplifier will have a phase shift of  $180^\circ$  and will be amplified.
- When a sinusoidal input is fed to non-inverting terminal and the inverting terminal is grounded, the output of the OP-AMP is only amplified without any phase shift.
- Positive feedback circuits are unstable circuits that add error and the already existing error. Hence negative feedback circuits are preferred. The negative feedback circuit provides stability to the circuit and corrects the error signal.

## NOTES

### 11.5 KEY WORDS

- **Operational amplifier:** It is multistage amplifier with direct coupling, having larger input resistance, higher gain and provided with small amount of negative feedback. It has very good stability and is operated with input signal frequency extending from 0 Hz to slightly greater than  $10^6$  Hz.
- **Inverting amplifier:** It is a normal OP-AMP having its non-inverting input connected to ground or common which introduces  $180^\circ$  phase shift between output voltage and input voltage.

### 11.6 SELF ASSESSMENT QUESTIONS AND EXERCISES

#### Short Answer Questions

1. Draw the IC 741 pin configuration and the circuit symbol of OP-AMP.
2. What is the need for  $V_{CC}$  and  $V_{EE}$  voltages in OP-AMP?
3. What do you understand by differential mode gain and common mode gain?

4. What are the advantages of negative feedback?
5. Draw the equivalent circuit of OP-AMP.

## NOTES

### Long Answer Questions

1. Explain the different pin configuration of OP-AMP IC 741.
2. What do you understand by the open loop and closed loop system in OP-AMP?
3. Explain the ideal characteristics of OP-AMP and relate it to the equivalent circuit of OP-AMP.

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## 11.7 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.

Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

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## UNIT 12 ELECTRICAL PARAMETERS OF OP-AMP

### NOTES

#### Structure

- 12.0 Introduction
- 12.1 Objectives
- 12.2 Non-Ideal OP-AMP Characteristics or Practical OP-AMP Characteristics
- 12.3 Input Capacitance of OP-AMP for Nullification
- 12.4 Answers to Check Your Progress
- 12.5 Summary
- 12.6 Key Words
- 12.7 Self Assessment Questions and Exercises
- 12.8 Further Readings

### 12.0 INTRODUCTION

Practical OP-AMPs have a higher degree of nonlinearity in the electrical parameters. For example, there exists an input current, though the input impedance of an ideal OP-AMP is infinity. Similarly, other electrical parameters such as input offset voltage, input bias current, input capacitance, output offset voltage, CMRR and slew rate will be discussed in this unit. The listed electrical parameters are nonideal characteristics of OP-AMP parameters that arise due to nonlinear internal transistors of OP-AMP.

### 12.1 OBJECTIVES

After going through this unit, you will be able to:

- Explain the various parameters of OP-AMP
- Discuss the input capacitance of OP-AMP for nullification

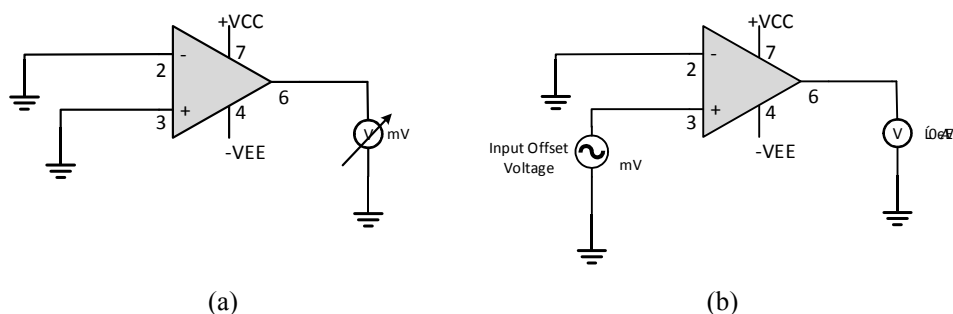
### 12.2 NON-IDEAL OP-AMP CHARACTERISTICS OR PRACTICAL OP-AMP CHARACTERISTICS

It is important to revisit the following ideal characteristics parameters of OP-AMP.

1. **Input Impedance:** Input impedance of practical OP-AMP are not infinite, but they have very large values in the range few  $M\Omega$ s to several hundred  $M\Omega$ .
2. **Output Impedance:** The output impedance of practical OP-AMP is not zero, but they are of very less values in the range of few  $10$ 's of ohms.

## NOTES

3. **Gain:** The gain of the practical amplifiers are never infinity but can be made to very large value by proper design of the feedback resistor,  $R_f$ . Practical gain may range from a few hundred to several thousands.
4. **Bandwidth:** Bandwidth is the range of frequencies in which the device operate satisfactorily for the desired performance. In the case of amplifiers, the desired performance is the process of amplification. Bandwidth for ideal amplifiers is infinity, whereas for the practical OP-AMPs with open loop circuit have the very small bandwidth. For closed loop OP-AMP circuits, bandwidth increase to a few decades ( $10^x$ ,  $x = 1, 2, 3 \dots$ ) of frequencies.
5. **Input Offset Voltage:** under ideal conditions, the output voltage must be zero, when no input voltage is applied. However, practically, there exists a small amount of output voltage even without applying any input voltage. This small output voltage may be due to the presence of bias voltages or due to the stored capacitance charges inside the OP-AMP employed to filter out noises and unwanted DC signals. In order to overcome the small output voltage, an equivalent small input voltage is applied to the inverting or non-inverting input terminals depending on the polarity of the output voltage. This small input voltage is known as input offset voltage.



**Fig. 12.1** (a) Input Offset "NULL" Voltage for OP-AMP (b) Input Offset Voltage for OP-AMP

6. **Input Bias Current:** The input inverting and non-inverting terminals are fed to two identical differential transistors  $Q_1$  and  $Q_2$  as shown in Figure 11.3. These two transistors must be identical for an ideal OP-AMP. But, practically, no two transistors can be identical due to various reasons such as manufacturing defect, materials used in transistors, etc.,. Also, for an ideal OP-AMP, the input differential transistors must offer infinite input resistance such that input current to the transistors are zero. But, in reality, there exists a small current of the order of few  $\mu A$ s that enters the input terminal of OP-AMP as shown in Figure 12.2. If bias currents across terminals are represented as  $I_{b1}$  and  $I_{b2}$ , normally, a manufacturer of OP-AMP specifies the average input bias current of the OP-AMP in their data sheet.

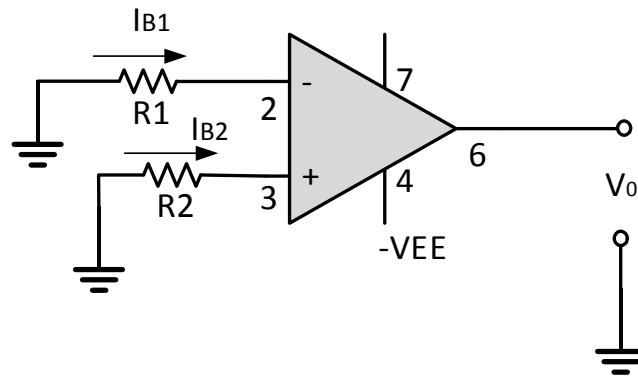


Fig. 12.2 Input Bias Current of an OP-AMP

The average bias current,  $I_b = \frac{(I_{b1} + I_{b2})}{2}$

- 7. Input Offset Current:** similar to the input offset voltage, the input additional current provided to a practical OP-AMP to reduce the small amount of output voltage is called as an input offset current. Ideally, the output voltage must be zero for zero input voltage and input current. But, since there exists a small output voltage, to offset the voltage to zero and to make the OP-AMP a balance device, an input offset current is provided at the input terminals. As shown in Figure 12.3, mathematically, input offset current is expressed as,

$$I_{oc} = I_{b2} - I_{b1}$$

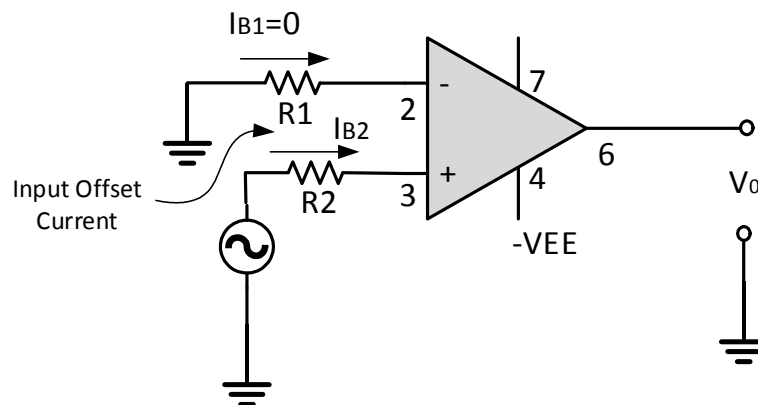


Fig. 12.3 Input Offset Current of OP-AMP

- 8. Output Offset Voltage:** In practical OP-AMPs, there exists an output voltage without any input voltage. This voltage is known as **output offset voltage** in OP-AMP. For an ideal OP-AMP, the output resistance is zero and hence the output voltage is equal to the  $A_{ol}V_d$ . Ideally,  $V_d$  must be zero, leading to the output voltage equal to zero ( $= A_{ol} \times 0$ ). The presence of

## NOTES



## NOTES

output voltage is due to the dissimilarities of the differential amplifier transistors. For a proper working of a differential amplifier, two transistors must be identical. But, practically, no two transistors can be identical.

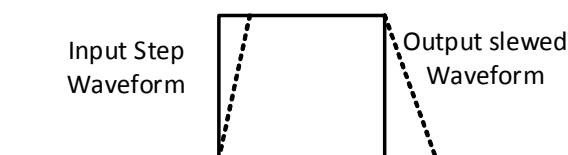
- 9. CMRR:** Common Mode Rejection Ratio or CMRR is defined as the ratio of differential gain,  $A_d$  to the common mode gain,  $A_{cm}$ . CMRR is the ability of the OP-AMP to reject the common signals that are available at the differential input of the OP-AMP. Two signals are said to be in common when they arrive at the same time and are in the same phase with each other. Ideally, CMRR must be infinity, whereas there exists a large value of CMRR, as the differential gain is not infinity, but a large value and the common mode gain is not zero, but a small value. Mathematically, CMRR is given as,

$$CMRR = \frac{A_d}{A_{cm}} \quad CMRR = \frac{\frac{V_0}{V_d}}{\frac{V_0}{V_{av}}} = \frac{V_{av}}{V_d} \quad CMRR = \frac{V_1 + V_2}{V_2 - V_1}$$

$$CMRR = \frac{V_1 + V_2}{2(V_2 - V_1)}$$

- 3. Slew Rate:** slew rate is defined as the rate of change in the output voltage for a step change in the input voltage. Ideally, slew rate must be infinity. That is, the change in the output voltage must have an immediate change when the input voltage is changed. For example, assume a step input voltage is given to the OP-AMP, the output voltage must also change instantly when the input changes from 0 to positive or negative voltage. But, practically, the instant change in output voltage does not happen. Mathematically, it is expressed as,

$$Slew\ Rate(SR) = \max\left(\frac{dV_0}{dt}\right)$$



**Fig. 12.4** Slew Rate of OP-AMP

### Summary of Ideal Characteristics of OP-AMP

Electrical Parameters of  
OP-AMP

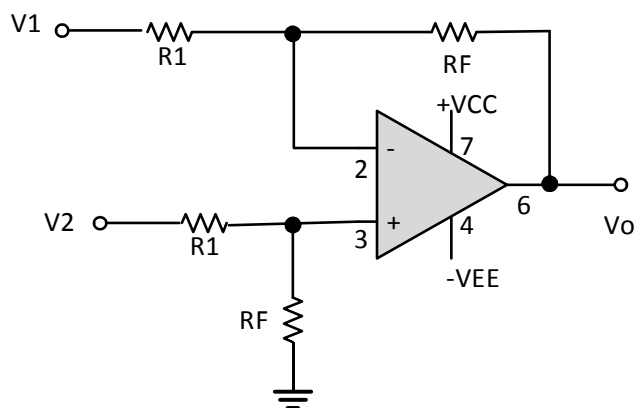
Characteristics of OP-AMP	Ideal Value
Input impedance	$Z_{in} = \infty$
Output Impedance	$Z_{out} = 0$
Gain	$A_{ol} = \infty$
Bandwidth	$BW = \infty$
CMRR	$CMRR = \infty$
Input offset voltage	$V_d = 0$
Output offset voltage	$V_0 = 0$
Input bias current	$I_b = 0$
Slew rate	$SR = \infty$

### NOTES

### 12.3 INPUT CAPACITANCE OF OP-AMP FOR NULLIFICATION

The instability of the OP-AMP may be compensated with external or internal compensation circuits. These compensation circuits are also called nullification circuits as they nullify the abnormalities of the electrical parameters due to manufacturing defects. OP-AMPs may be categorized based on the compensation circuits employed. They are either uncompensated or internally compensated. Uncompensated OP-AMPs always require external compensation components to achieve stability; while internally compensated OP-AMPs are stable, under limited conditions, with no additional external components. Internally compensated OP-AMPs can become unstable in several ways: by driving capacitive loads, by adding capacitance to the inverting input terminal and adding feedback with external components. This feedback must be such that they are in-phase with the input circuit. Adding in-phase feedback is a popular method of compensation. However, this method is out of the scope for this text. The effect of input capacitance on stability is hard to avoid because the OP-AMP terminals have stray capacitances and multiple conducting lines also contribute to unavoidable shunt capacitance. Hence, many internally compensated OP-AMP circuits require external compensation to restore stability. The stability of the circuit is determined by the gain-bandwidth product  $A\beta$ . Consider the circuit shown in Figure 12.5. The term,  $\beta$  is the feedback gain, the forward open loop gain is  $A$ . Therefore,  $A\beta$  for the circuit is given as,

## NOTES

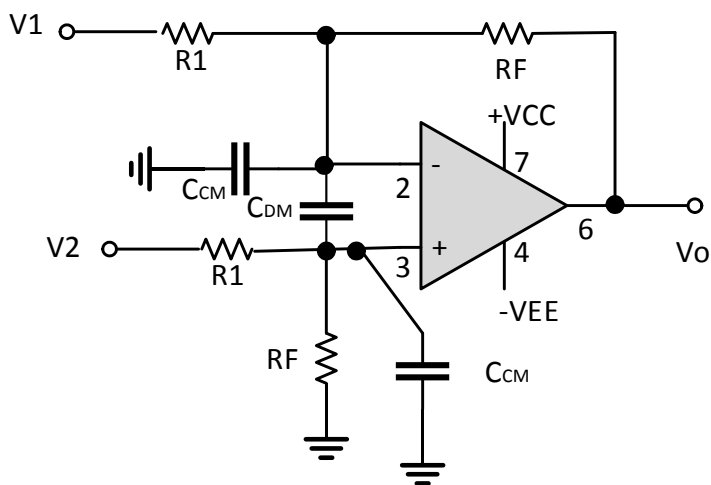


**Fig. 12.5** An Example Circuit of an OP-AMP

$$A\beta = \frac{A_{ol}R_1}{R_1 + R_f}$$

Where  $A_{ol}$ , is the open loop gain.

The above circuit also contains differential capacitance and common mode capacitance as shown in Figure 12.6. The differential mode capacitance is represented as  $C_{DM}$  and the common mode capacitance is represented as  $C_{CM}$ . On including all, the input capacitors for the analysis of stability of the circuit, the loop gain for the circuit modifies to the following expression.

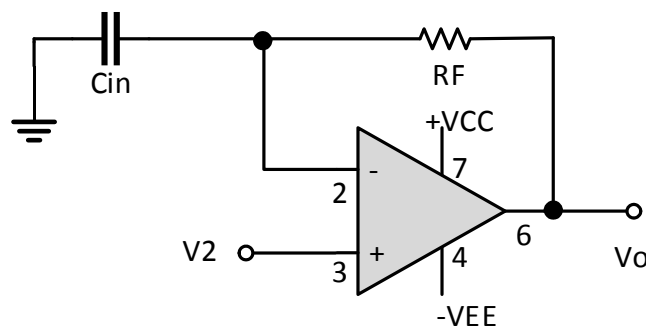


**Fig. 12.6** Slew Rate of OP-AMP

$$A\beta = \frac{A_{ol}R_1}{R_1 + R_f} \times \frac{1}{R_1 \parallel R_f C_{in} + 1}$$

The capacitor  $C_{in}$  includes the common mode, differential mode capacitances and stray capacitances of the circuit. Input capacitors and the output capacitors affect the stability of the circuit to a great extent. And hence, a compensation capacitance,  $C_{in}$  that include all internal and external capacitances is included in the circuit as an external compensator. The stability of the circuit is greatly improved by the configuration shown in Figure 12.7. The loop gain of such a circuit is given as:

$$A\beta = \frac{A_{ol}}{(R_f + R_o)C_{in} + 1}$$



**Fig. 12.7** Externally Compensated OP-AMP Circuit

### Check Your Progress

1. Define input offset voltage.
2. Define input offset current.
3. What is slew rate?

## 12.4 ANSWERS TO CHECK YOUR PROGRESS

1. Under ideal conditions, the output voltage must be zero, when no input voltage is applied. However, practically, there exists a small amount of output voltage even without applying any input voltage. In order to overcome the small output voltage, an equivalent small input voltage is applied to the inverting or non-inverting input terminals depending on the polarity of the output voltage. This small input voltage is known as input offset voltage.
2. Similar to the input offset voltage, the input additional current provided to a practical OP-AMP to reduce the small amount of output voltage is called as an input offset current.
3. Slew rate is defined as the rate of change in the output voltage for a step change in the input voltage.

## NOTES

## NOTES

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### 12.5 SUMMARY

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- The gain of the practical amplifiers are never infinity but can be made to very large value by proper design of the feedback resistor.
- Bandwidth is the range of frequencies in which the device operate satisfactorily for the desired performance.
- In order to overcome the small output voltage, an equivalent small input voltage is applied to the inverting or non-inverting input terminals depending on the polarity of the output voltage. This small input voltage is known as input offset voltage.
- Similar to the input offset voltage, the input additional current provided to a practical OP-AMP to reduce the small amount of output voltage is called as an input offset current.
- The instability of the OP-AMP may be compensated with external or internal compensation circuits. These compensation circuits are also called nullification circuits as they nullify the abnormalities of the electrical parameters due to manufacturing defects.

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### 12.6 KEY WORDS

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- **Common Mode Rejection Ratio (CMRR):** It is defined as the ratio of differential gain to the common mode gain.
- **Slew Rate (SR):** It is defined as the rate of change in the output voltage for a step change in the input voltage.

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### 12.7 SELF ASSESSMENT QUESTIONS AND EXERCISES

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#### Short Answer Questions

1. Define CMRR.
2. Mention the ideal OP-AMP characteristics.
3. What do you understand by input bias current?
4. Mention the importance of common mode gain and differential mode gain.
5. Define the gain-bandwidth product.

#### Long Answer Questions

1. Explain the effect of identical differential transistors in OP-AMP.
2. Describe in detail the stability of OP-AMP due to the capacitances.

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## 12.8 FURTHER READINGS

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Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.

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Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.

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*Electrical Parameters of  
OP-AMP*

## NOTES

## NOTES

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# UNIT 13 APPLICATIONS OF OP-AMO

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### Structure

- 13.0 Introduction
- 13.1 Objectives
- 13.2 Applications of OP-AMP
  - 13.2.1 Inverting Amplifiers
  - 13.2.2 Non-Inverting Amplifier
  - 13.2.3 Adder
  - 13.2.4 Subtractor
  - 13.2.5 Differentiator
  - 13.2.6 Integrator
  - 13.2.7 Log Amplifier
  - 13.2.8 Antilog Amplifier
  - 13.2.9 Comparator
- 13.3 Answers to Check Your Progress
- 13.4 Summary
- 13.5 Key Words
- 13.6 Self Assessment Questions and Exercises
- 13.7 Further Readings

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## 13.0 INTRODUCTION

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You have already learnt the internal architecture of OP-AMP, their electrical behavior, and the instability issues. Also, so far the contrasting behavior of ideal assumptions and the practical reality of OP-AMP has discussed. Considering the ideal OP-AMP, you will learn about the different applications of OP-AMP in the real-world scenario. Discussing the applications for a non-ideal OP-AMP will complicate the understanding of OP-AMP applications and hence such analysis is out of scope of syllabus. Applications of OP-AMP such as an inverting amplifier, non-inverting amplifier, adders, subtractor, integrators, differentiators etc. will be discussed in this unit.

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## 13.1 OBJECTIVES

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After going through this unit, you will be able to:

- Explain the linear and non-linear applications of OP-AMP
- Derive the expression for output voltage of OP-AMP applications
- Understand the input and output waveforms

## 13.2 APPLICATIONS OF OP-AMP

In general, the applications of OP-AMP can be classified as linear applications and non-linear applications. In applications such as a differential amplifier, inverting and non-inverting amplifiers, instrumentation amplifiers, buffer amplifiers etc., the output voltage and input voltage are linear to each other with a difference in the gain parameter. Such applications are categorized as linear applications.

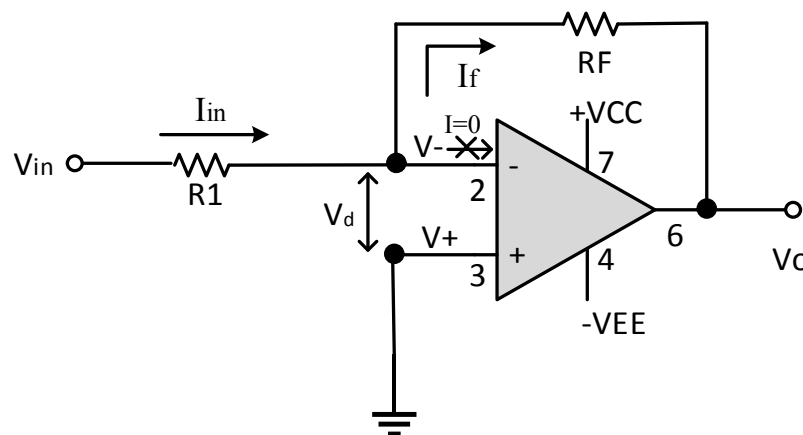
Non-linear applications of OP-AMP include clippers, clampers, log amplifiers, antilog amplifiers, Schmitt trigger, series and shunt regulators etc., the nonlinearity is based on the type of feedback element used in the feedback circuit. When nonlinear elements like a diode, transistors are used in the feedback circuit of OP-AMP, then they are categorized as a part of non-linear applications of OP-AMP.

OP-AMP are used in following analog mathematical applications:

- Inverting Amplifiers
- Non-inverting Amplifiers
- Adders
- Subtractor
- Differentiator
- Integrator
- Log amplifiers
- Antilog Amplifiers

### 13.2.1 Inverting Amplifiers

Amplifiers that invert the input signal and amplifies are called as inverting amplifiers. The input and output signals are anti-phase with each other. They exhibit a phase difference of  $180^\circ$ . The basic circuit diagram of the inverting amplifier is given in Figure 13.1.



**Fig. 13.1** Inverting Amplifier

## NOTES



## NOTES

The inverting amplifier circuit shown in Figure 13.1 consists of input voltage fed only to the inverting input terminal of OP-AMP. The non-inverting terminal input is grounded. There exists a negative feedback resistor connected between the inverting terminal and the output terminal. The output voltage is  $V_0$ , seen across the output terminal pin 6 of IC 741. The bias voltages are  $V_{CC}$  and  $V_{EE}$  supplied to the pins  $V_{sat}$  and  $-V_{sat}$  respectively of IC 741. Based on the ideal characteristics of OP-AMP following observations are important before analysing the circuit.

- $I = 0$ . The input current to the amplifier is zero. According to ideal OP-AMP characteristics, since the input resistance is infinity, such huge resistance does not allow any current into the differential amplifier.
- The difference voltage,  $V_d = 0$ . Since the ideal differential amplifiers are identical and also, since the input resistance is infinite, the inverting terminal voltage  $V^-$  and the non-inverting terminal voltage  $V^+$  are equal.

Therefore,  $V^- = V^+ \quad V_d = V^+ - V^- = 0V$

### The Expression for Output Voltage

From Figure 13.1,

$$V^+ = 0V$$

Since,

$$V^+ = V^- = 0V$$

The input current,

$$I_{in} = \frac{V_{in} - V^-}{R_1} = \frac{V_{in}}{R_1}$$

The feedback current,

$$I_f = \frac{V^- - V_0}{R_f} = \frac{-V_0}{R_f}$$

$$\text{Applying KCL at } V^-, \quad I_{in} = I_f \quad \frac{V_{in}}{R_1} = \frac{-V_0}{R_f}$$

$$V_0 = -\frac{R_f}{R_1} V_{in}$$

$$A_v = \frac{V_0}{V_{in}} = -\frac{R_f}{R_1}$$

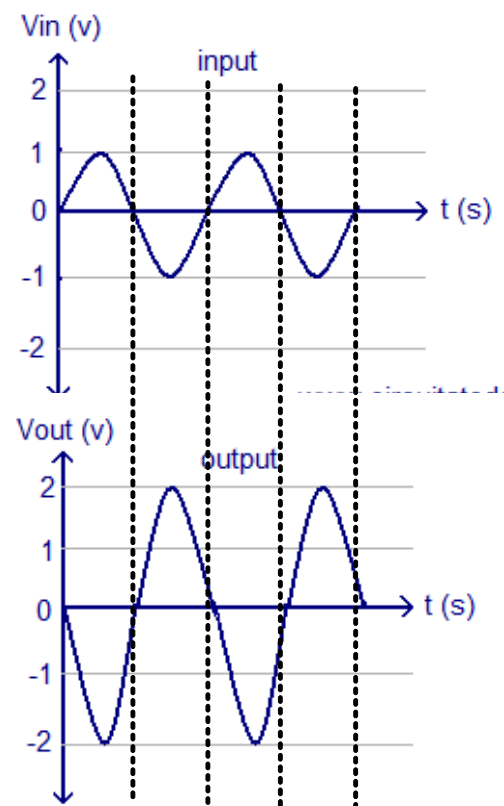
From the output expression for the inverting amplifier, it is evident that the output voltage and input voltage are linearly proportional. The input voltage is amplified with a gain equivalent to  $R_f / R_1$ . The negative sign indicates that the output voltage is an inverted form of the input voltage. The feedback resistor  $R_f$ , plays an important role in determining the magnitude of the gain. Large the value of  $R_f$ , larger is the input voltage amplification.

It should also be observed that the voltage gain depends on the ratio of the feedback resistor to the input resistor.

- If  $R_f \gg R_1$ , gain,  $A_v \gg 1$
- If  $R_f < R_1$ , gain,  $A_v < 1$
- If  $R_f = R_1$ , gain,  $A_v = 1$

The above circuit when  $R_f = R_1$ , is known is phase inverter, since  $A_v = 1$ , therefore,  $V_o = -V_{in}$ .

The input-output waveforms are given in Figure 13.2.



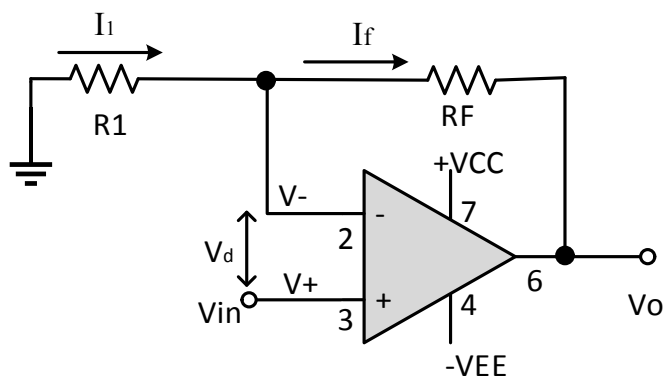
**Fig. 13.2** Input-Output Waveforms of an Inverting Amplifier ( Gain is Assumed to be 2)

## NOTES

## NOTES

### 13.2.2 Non-Inverting Amplifier

In non-inverting amplifiers, the input voltage is not inverted but only amplified. The gain of the amplifier gets modified and is always greater than 1. The circuit diagram of a non-inverting amplifier is given in Figure 13.3.



**Fig. 13.3** Non-Inverting Amplifier

The non-inverting amplifier consists of input fed to the non-inverting terminal pin 3 of IC 741. The inverting terminal is connected to ground through a resistance  $R_1$ . The negative feedback from the output is fed to the inverting terminal.

#### Derivation of Output Voltage

From Figure 13.3,

$$V^+ = V_{in}$$

Since,

$$V_d = V^+ - V^- = 0$$

$$V^+ = V^- = V_{in}$$

The input current,

$$I_1 = \frac{0 - V^-}{R_1} = \frac{-V^-}{R_1} = -\frac{V_{in}}{R_1}$$

The feedback current,

$$I_f = \frac{V^- - V_o}{R_f} = \frac{V_{in} - V_o}{R_f}$$

Applying KCL at  $V^-$ ,

$$I_1 = I_f - \frac{V_{in}}{R_1} = \frac{V_{in} - V_o}{R_f} - \frac{V_{in}}{R_1} = \frac{V_{in}}{R_f} - \frac{V_o}{R_f}$$

$$\frac{V_0}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1}$$

$$\frac{V_0}{R_f} = \frac{V_{in}}{R_f} + \frac{V_{in}}{R_1} = V_{in} \left( \frac{1}{R_f} + \frac{1}{R_1} \right)$$

$$\frac{V_0}{R_f} = V_{in} \left( \frac{R_f + R_1}{R_f R_1} \right)$$

$$V_0 = V_{in} \left( \frac{R_f + R_1}{R_f R_1} \right) \times R_f$$

$$V_0 = V_{in} \left( \frac{R_f + R_1}{R_1} \right)$$

$$V_0 = \left( 1 + \frac{R_f}{R_1} \right) V_{in}$$

$$A_v = \frac{V_0}{V_{in}} = 1 + \frac{R_f}{R_1}$$

From the above output expression, the output voltage is not an inverted signal of the input voltage due to the absence of the negative terminal. But, the output voltage is a product of input voltage and an amplification factor equivalent

to  $1 + \frac{R_f}{R_1}$ . The voltage gain of the non-inverting amplifier is  $1 + \frac{R_f}{R_1}$ .

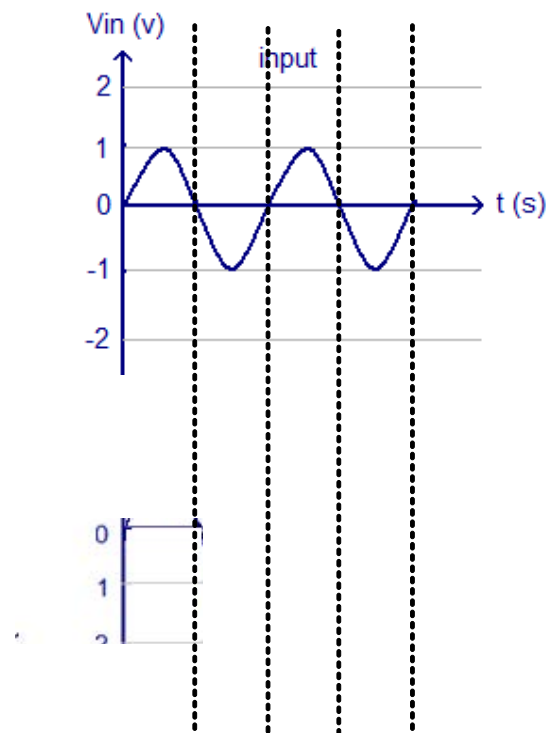
Also, it should be noted that gain for a non-inverting amplifier is always greater than 1. That is,

- If  $R_f > R_1$ , gain,  $A_v > 1$
- If  $R_f < R_1$ , gain,  $A_v > 1$
- If  $R_f = R_1$ , gain,  $A_v = 2$

The input-output waveform of the non-inverting amplifier is given in Figure 13.4.

## NOTES

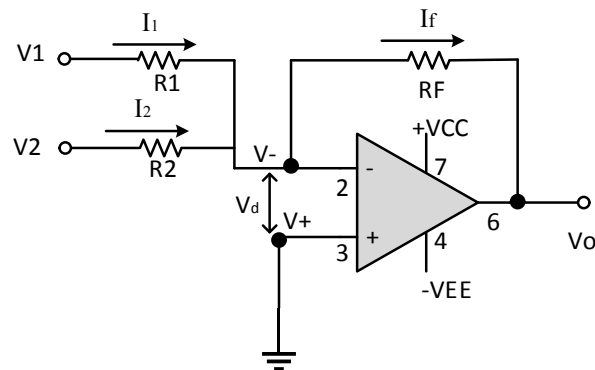
## NOTES



**Fig. 13.4** Input-Output Waveforms of a Non-Inverting Amplifier  
(Gain is Assumed to be 2)

### 13.2.3 Adder

OP-AMPs may be used to perform mathematical operations such as addition and subtraction. The input voltage signals to be added are fed to either inverting or non-inverting input terminal. The circuit diagram for adder is shown in Figure 13.5. The adder circuit consists of two input voltages,  $V_1$  and  $V_2$  to be added. Input current  $I_1$  and  $I_2$  flows across  $R_1$  and  $R_2$ . The non-inverting terminal is grounded. The feedback from output to inverting input terminal is fed through feedback resistor  $R_f$ .



**Fig. 13.5** Adder using OP-AMP

**Derivation of Output Voltage**

From Figure 13.5,

$$V^+ = 0$$

Since,

$$V_d = V^+ - V^- = 0$$

$$V^+ = V^- = 0$$

The input current,

$$I_1 = \frac{V_1 - V^-}{R_1} = \frac{V_1}{R_1}$$

$$I_2 = \frac{V_2 - V^-}{R_2} = \frac{V_2}{R_2}$$

The feedback current,

$$I_f = \frac{V^- - V_0}{R_f} = \frac{-V_0}{R_f}$$

$$\text{Applying KCL at } V^-, I_1 + I_2 = I_f \quad \frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{-V_0}{R_f}$$

$$\text{Let } R_1 = R_2 = R, \quad \frac{V_1}{R} + \frac{V_2}{R} = \frac{-V_0}{R_f} \quad \frac{1}{R}(V_1 + V_2) = \frac{-V_0}{R_f}$$

$$V_0 = -\frac{R_f}{R}(V_1 + V_2)$$

Thus from the above output expression, the output voltage is a sum of input voltages for the given configuration of the OP-AMP circuit shown in Figure 13.5.

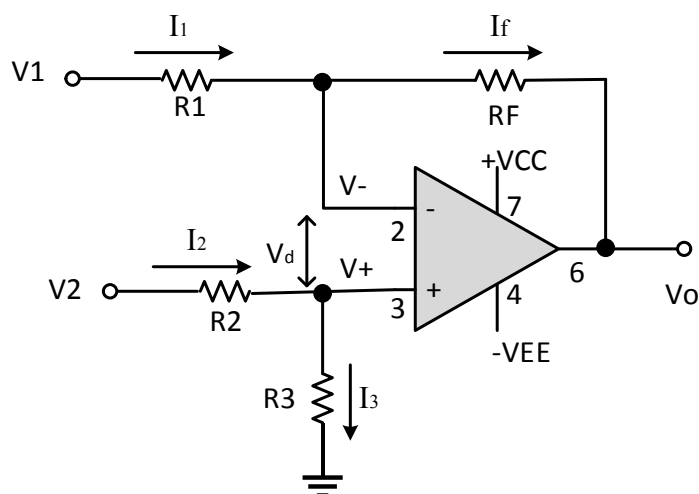
The ratio,  $R_f / R$  is the scaling factor. The negative sign indicates that the sum of input voltages will be inverted. This is due to the fact that both the input voltages are fed to the inverting terminal of the OP-AMP.

**13.2.4 Subtractor**

The subtractor circuit using OP-AMP is shown in Figure 13.6. The output voltage will be a difference of both the input voltages.

**NOTES**

## NOTES



**Fig. 13.6** Subtractor using OP-AMP

One input voltage to the subtractor circuit is fed to the non-inverting terminal and the other input to be subtracted is fed to the inverting terminal of the OP-AMP. The feedback resistance  $R_f$  is connected between the output terminal and the inverting terminal.

### Derivation of Output Voltage

We know that,

$$V_d = V^+ - V^- = 0$$

Therefore,

$$V^+ = V^-$$

Applying voltage divider rule

$$V^+ = V_2 \frac{R_3}{R_2 + R_3}$$

$$\therefore V^- = V^+ = V_2 \frac{R_3}{R_2 + R_3}$$

The input currents are given as,

$$I_1 = \frac{V_1 - V^-}{R_1} = \frac{V_1}{R_1} - \frac{1}{R_1} \left( V_2 \frac{R_3}{R_2 + R_3} \right)$$

The feedback current,

$$I_f = \frac{V^- - V_o}{R_f} = \frac{1}{R_f} \left( V_2 \frac{R_3}{R_2 + R_3} \right) - \frac{V_o}{R_f}$$

Applying KCL at  $V^-$ ,

$$I_1 = I_f \frac{V_1}{R_1} - \frac{1}{R_1} \left( V_2 \frac{R_3}{R_2 + R_3} \right) = \frac{1}{R_f} \left( V_2 \frac{R_3}{R_2 + R_3} \right) - \frac{V_0}{R_f}$$

Let  $R_1 = R_2 = R_3 = R_f = R$ , then

$$\frac{V_1}{R} - \frac{1}{R} \left( V_2 \frac{R}{2R} \right) = \frac{1}{R} \left( V_2 \frac{R}{2R} \right) - \frac{V_0}{R} \frac{V_1}{R} - \frac{1}{R} \left( V_2 \frac{1}{2} \right) = \frac{1}{R} \left( V_2 \frac{1}{2} \right) - \frac{V_0}{R}$$

$$\frac{V_0}{R} = \frac{V_2}{2R} - \frac{V_1}{R} + \frac{V_2}{2R}$$

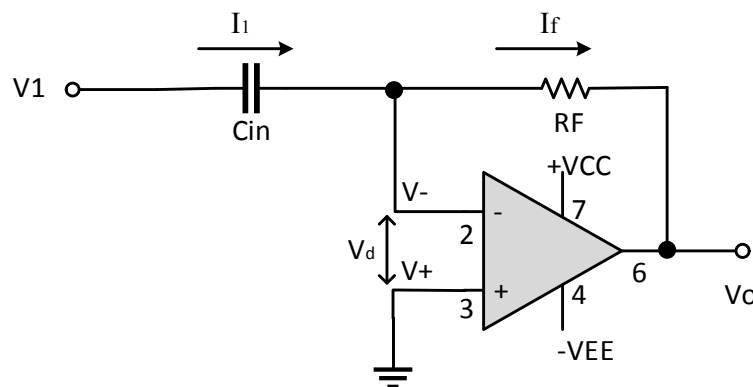
$$V_0 = R \left( \frac{V_2}{R} - \frac{V_1}{R} \right)$$

$$V_0 = V_2 - V_1$$

Thus, it is evident that the output voltage is a difference between the two input voltage. It is to be noted that  $V_2$  is applied to the non-inverting terminal and  $V_1$  is applied to the inverting terminal. Also, by proper choice of the ratio  $R_f / R$ , the scaling factor for each input voltage may vary and accordingly, the difference amplifier may be fine tuned.

### 13.2.5 Differentiator

Another important application of OP-AMPS is it can be used to perform mathematical differentiation of an input signal. The circuit diagram to perform the differentiator is shown in Figure 13.7.



**Fig. 13.7** Differentiator using OP-AMP

## NOTES



## NOTES

The input signal is connected to the inverting terminal through an input capacitor  $C_{in}$ . The non-inverting terminal is grounded and the feedback network consist of a feedback resistor connected between the output terminal and inverting terminal.

### Derivation of Output Voltage

From Figure 13.7,

$$V^+ = 0$$

Since,

$$V_d = V^+ - V^- = 0$$

$$V^+ = V^- = 0$$

The input current,

$$I_1 = C_{in} \frac{d(V_1 - V^-)}{dt} = C_{in} \frac{d(V_1 - 0)}{dt} = C_{in} \frac{dV_1}{dt}$$

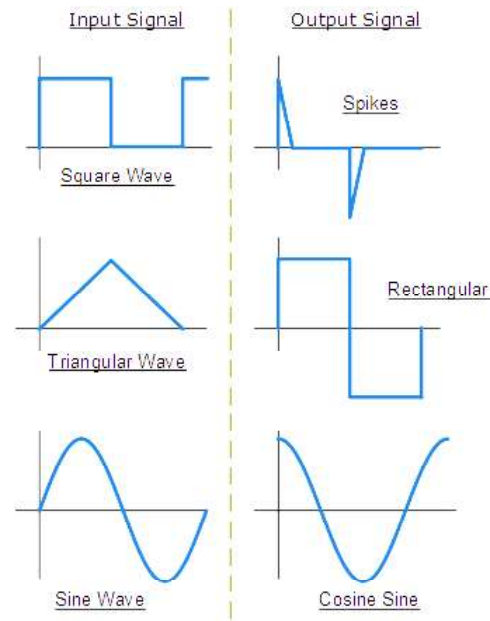
$$I_f = \frac{V^- - V_0}{R_f} = \frac{-V_0}{R_f}$$

$$\text{Applying, KCL at } V^-, I_1 = I_f \quad C_{in} \frac{dV_1}{dt} = \frac{-V_0}{R_f}$$

Therefore,

$$V_0 = -C_{in} R_f \frac{dV_1}{dt}$$

Thus from the above expression, the output voltage is differential of the input voltage. The negative sign in the expression is due to the input signal being provided to the inverting terminal of OP-AMP. The gain factor or scaling factor is  $C_{in} R_f$ . The input-output waveform for a differentiator circuit is given in Figure 13.8. It is evident that the differential of sine is cosine, a differential of the ramp signal is a constant and differential of a constant is zero. This such differential circuits are used in most mathematical functions.

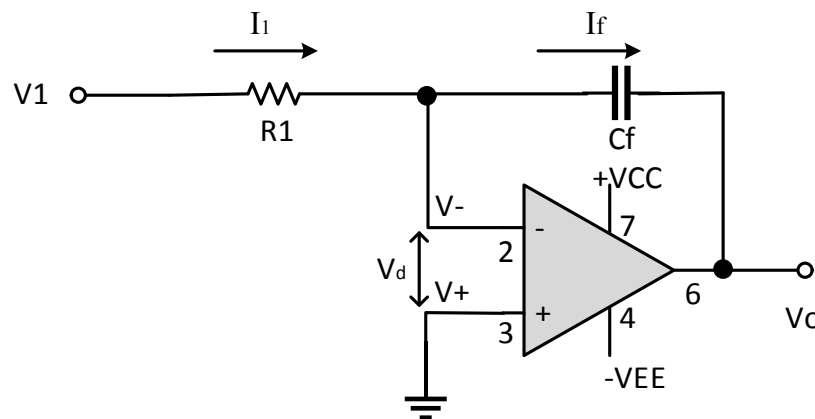


**Fig. 13.8** Input-Output Waveforms for a Differentiator

## NOTES

### 13.2.6 Integrator

Another important application of OP-AMP is as a mathematical function integrator. The output voltage of an OP-AMP is an integral function of the input voltage. This is achieved by replacing the capacitance in the input side of the differentiator circuit to the feedback network. The integrator circuit is as shown in Figure 13.9.



**Fig. 13.9** Integrator using OP-AMP

The integrator circuit consists of input resistance  $R_1$  connected to the input voltage and the capacitor forms a part of the negative feedback circuit. Non-inverting terminal is grounded. This circuit may also be called as an inverting integrator, since the input voltage is connected to the inverting terminal of the OP-AMP.

## Derivation of the Output Voltage

From Figure 13.9,

$$V^+ = 0$$

Since,

$$V_d = V^+ - V^- = 0$$

$$V^+ = V^- = 0$$

The input current,

$$I_1 = \frac{V_1 - V^-}{R_1} = \frac{V_1}{R_1}$$

The feedback current,

$$I_f = C_f \frac{d(V^- - V_0)}{dt} = C_f \frac{-d(V_0)}{dt}$$

Applying KCL at  $V^-$ ,

$$I_1 = I_f$$

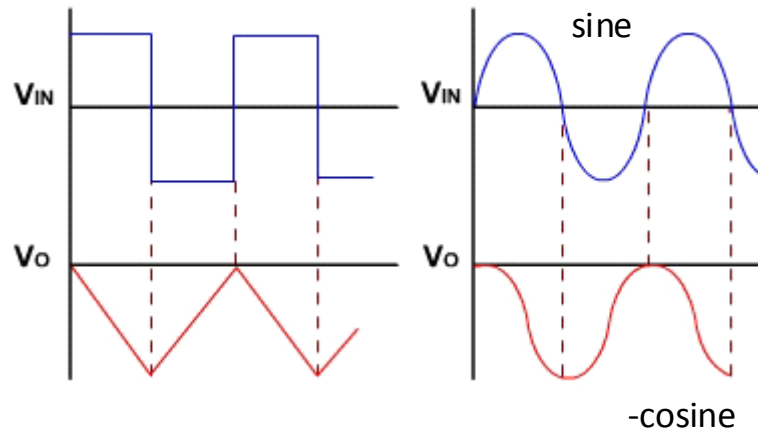
$$\frac{V_1}{R_1} = C_f \frac{-d(V_0)}{dt}$$

$$\frac{d(V_0)}{dt} = -\frac{1}{R_1 C_f} V_1 V_0 = -\frac{1}{R_1 C_f} \int V_1 dt$$

Thus from the above output voltage expression of the integrator, it is evident

that the output voltage is an integral of the input voltage. The ratio  $\frac{1}{R_1 C_f}$  is the scaling factor of the integral of the input voltage. The input-output wave form for an integrator circuit is shown in Figure 13.10. When an input voltage is a square waveform, the output of the integrator circuit is a triangular waveform, since integral of the constant value is a linear function of t, if operated in time domain function. Similarly, integral of sine is –cosine and hence the waveform is as shown in Figure 13.10.

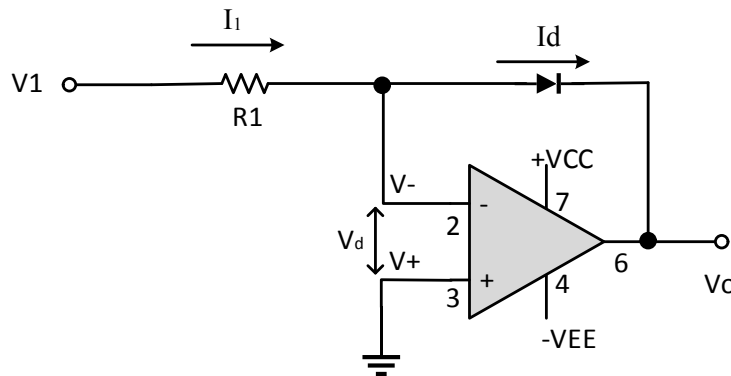
### NOTES



**Fig. 13.10** Input-Output Waveforms of Integrator

### 13.2.7 Log Amplifier

OP-AMPs may also be used as logarithmic amplifiers. Such amplifiers are nonlinear applications of OP-AMP. They employ diode in the negative feedback circuit. It is important to recall the diode equation to analyze the derivation of a log amplifier. In the log amplifier, the output voltage is a logarithmic function of the input voltage. The log amplifier is as shown in Figure 13.11. The derivation of the output voltage is similar to the earlier derived approaches. The non-inverting terminal is grounded and the inverting terminal is fed with input voltage through resistance  $R_1$ . A diode forms the feedback circuit connected in forward bias between the inverting terminal and the output terminal.



**Fig. 13.11** Log Amplifier using OP-AMP

### Derivation of Output Voltage

From Figure 13.11,

$$V^+ = 0$$

## NOTES

## NOTES

Since,

$$V_d = V^+ - V^- = 0$$

$$V^+ = V^- = 0$$

The input current,

$$I_1 = \frac{V_1 - V^-}{R_1} = \frac{V_1}{R_1}$$

The feedback diode forward biased current,

$$I_d = I_0 e^{V_d / \eta V_T}$$

Where the diode voltage  $V_d$  is given by,  $V_d = V^- - V_0$   $V_d = -V_0$

Applying KCL at  $V^-$ ,  $I_1 = I_d$   $\frac{V_1}{R_1} = I_0 e^{\frac{V_d}{\eta V_T}}$

Substituting for  $V_d$  and rearranging,

$$e^{\frac{-V_0}{\eta V_T}} = \frac{V_1}{R_1 I_0} \frac{-V_0}{\eta V_T} = \ln \left[ \frac{V_1}{R_1 I_0} \right] V_0 = -\eta V_T \ln \left[ \frac{V_1}{R_1 I_0} \right]$$

Thus, the output voltage is a logarithmic function of the input voltage.

### 13.2.8 Antilog Amplifier

Similar to various mathematical applications linear and nonlinear applications of OP-AMP, antilog amplifier is another nonlinear application of OP-AMP. The output voltage is an antilog function of the input voltage. Following the similar approach of determining the output voltage expression of OP-AMP, we have the following.

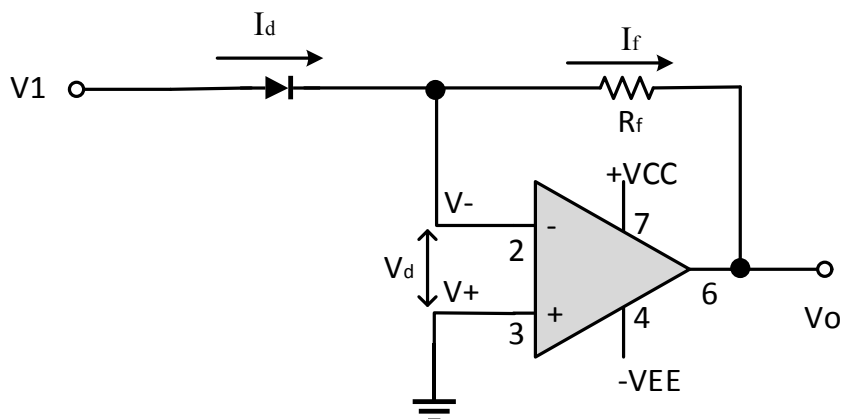


Fig. 13.12 Antilog Amplifier using OP-AMP

**Derivation of Output Voltage**

From Figure 13.12,  $V^+ = 0$

Since,  $V_d = V^+ - V^- = 0$   $V^+ = V^- = 0$

The diode input current,  $I_d$  is given as

$$I_d = I_0 e^{V_d / \eta V_T}$$

Where the diode voltage  $V_d$  is given by,

$$V_d = V_1 - V^- \quad \because V^- = 0 \quad V_d = V_1$$

Therefore,

$$I_d = I_0 e^{V_1 / \eta V_T}$$

Also, the feedback current is given as,

$$I_f = \frac{V^- - V_0}{R_f} = -\frac{V_0}{R_f}$$

Applying KCL at  $V^-$ ,

$$I_d = I_f \quad I_0 e^{V_1 / \eta V_T} = -\frac{V_0}{R_f} \quad V_0 = -R_f I_0 e^{V_1 / \eta V_T}$$

Thus, it is observed that the output voltage is an antilogarithmic function or exponential function of input voltage,  $V_1$ . Log and antilog amplifiers can also be constructed by replacing the diodes with transistors.

**13.2.9 Comparator**

The function of the comparator is that two input signals are compared by the OP-AMP input terminals, the output is a square pulse representing the greater voltage of the input signal. In comparator, the amplifier is forced to work in saturation mode. There are two types of OP-AMP comparator circuits. They are open loop comparators and closed loop comparators.

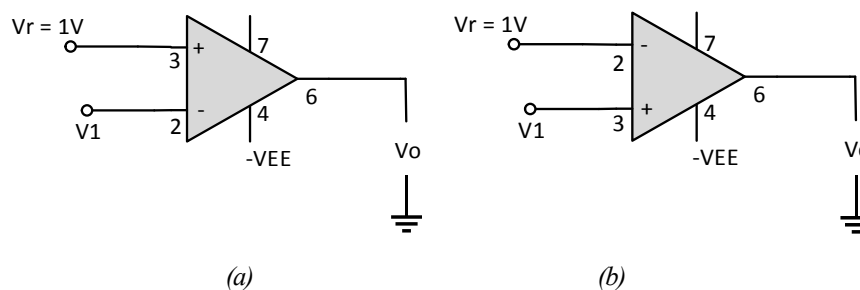
Open loop comparators do not have feedback, whereas the closed loop comparators have a negative feedback. Open loop comparators may be inverting comparators or non-inverting comparators.

**Open Loop Comparators**

Open loop comparators employ OP-AMP without any feedback, and hence the gain of the OP-AMP is an open loop gain,  $A_{ol}$ . The circuit diagram is shown in Figure 13.13.

**NOTES**

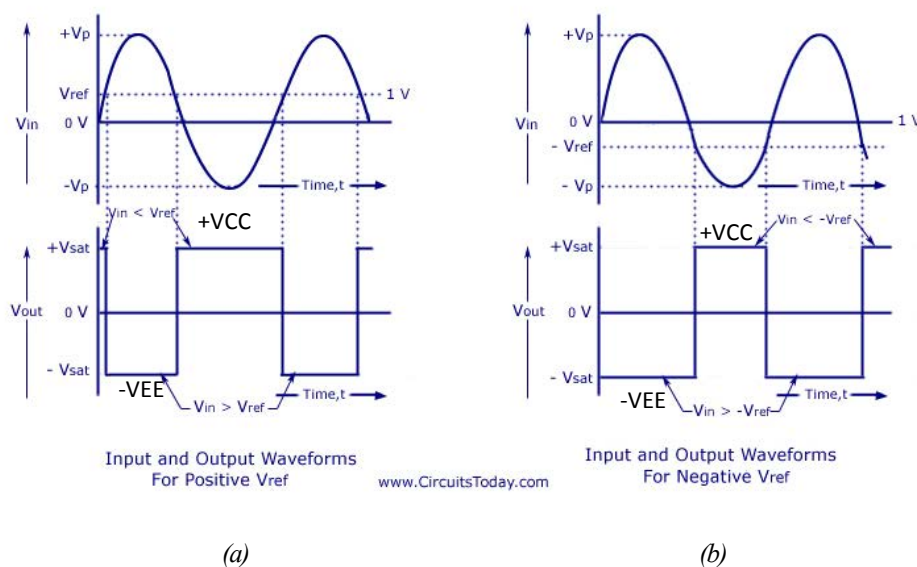
## NOTES



**Fig. 13.13** Open Loop Comparator (a) Inverting (b) Non-Inverting

### Inverting Comparators

In inverting comparator, the input signal is provided to the inverting terminal and the non-inverting is provided with a reference voltage,  $V_r \geq 0V$ . Inverting comparators provide a positive reference voltage,  $+V_r$ , since the reference voltage is fed to the non-inverting terminal of the OP-AMP. Since the given configuration is an open loop configuration, the open loop gain,  $A_{ol} \gg 1$ . Hence, even a slightest input voltage,  $V_{in} > V_r$ , drives the OP-AMP to saturation. The driven positive saturation voltage,  $V_{sat}$  is equal to  $+V_{CC}$ . The input-output waveform for an inverting comparators is given in Figure 13.14 (a). the negative saturation voltage is  $-V_{sat} \equiv -V_{EE}$ .



**Fig. 13.14** Input-Output Waveforms of Open-Loop Comparator  
(a) Inverting (b) Non-Inverting

When the input voltage,  $V_{in}$  is greater than  $V_r$ , the output voltage is driven to the saturated voltage  $V_{sat} = +V_{CC}$  and when the input voltage,  $V_{in}$  is less than  $V_r$ , the output voltage is driven to the negative saturated voltage  $-V_{sat} = -V_{EE}$ .

## NOTES

### Non-Inverting Comparators

In non-inverting comparators, the input signal is provided to the non-inverting terminal and the inverting terminal is provided with a reference voltage,  $V_r \geq 0V$ . Since, the reference voltage is a negative voltage, whenever the input voltage is driven more negative than  $V_r$ , the output voltage is driven to  $+V_{sat} = +V_{CC}$ . Whenever the input voltage is less than the negative reference voltage, the output voltage is driven  $-V_{sat} = -V_{EE}$ . The input-output waveform is shown in Figure 13.14 (b).

### Feedback Comparators or Schmitt Trigger

Similar to open loop comparators, there exists an inverting Schmitt trigger and non-inverting Schmitt trigger. A simple inverting Schmitt trigger circuit is shown in Figure 13.15. The inverting input terminal is provided with an input voltage  $V_i$  and the non-inverting terminal is fed with a feedback network consisting of a potential divider network  $R_1$  and  $R_2$ . The output voltage is across the two feedback resistors.

The voltage across resistor  $R_1$  is the reference voltage,  $V_r$ . The reference voltage determines the saturation level of the Schmitt trigger circuit. As discussed earlier, whenever, the input voltage,  $V_i > V_r$ , the output voltage is equal to  $+V_{sat}$  and when  $V_i < V_r$ , the output voltage is equal to  $-V_{sat}$ .

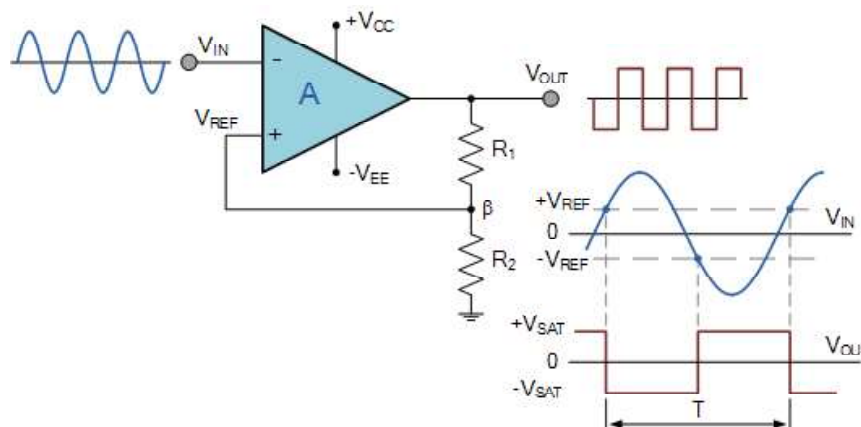


Fig. 13.15 Schmitt Trigger



## NOTES

The reference voltage by applying the voltage divider rule,  
The reference voltage by applying the voltage divider rule,

$$+V_r = V_0 \frac{R_1}{R_1 + R_2} = V_{sat} \frac{R_1}{R_1 + R_2}, \text{ for positive saturation}$$

Similarly,

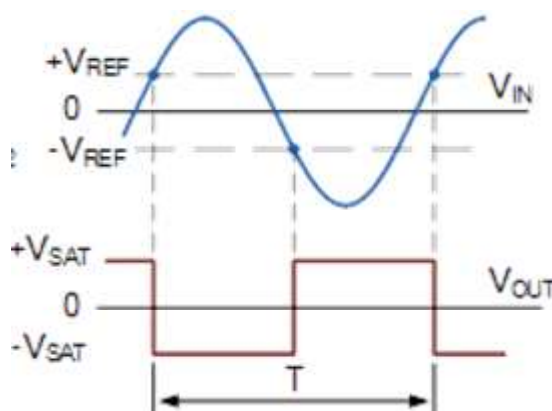
$$-V_r = V_0 \frac{R_1}{R_1 + R_2} = -V_{sat} \frac{R_1}{R_1 + R_2}, \text{ for negative saturation}$$

The positive reference voltage,  $+V_r$  is also called as upper threshold voltage,  $V_{UT}$  and the negative reference voltage,  $-V_r$  is also called as lower threshold voltage,  $V_{LT}$ . Hence, mathematically, it is given as

$$V_{UT} = V_{sat} \frac{R_1}{R_1 + R_2}$$

$$V_{LT} = -V_{sat} \frac{R_1}{R_1 + R_2}$$

The input-output waveform of a Schmitt trigger is as shown in Figure 13.16.



**Fig. 13.16** Input-Output Waveforms of Schmitt Trigger

### Check Your Progress

1. What are linear applications of OP-AMP?
2. What are inverting amplifiers?
3. What are the two types of comparators?

---

### 13.3 ANSWERS TO CHECK YOUR PROGRESS

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1. In applications such as a differential amplifier, inverting and non-inverting amplifiers, instrumentation amplifiers, buffer amplifiers etc., the output voltage and input voltage are linear to each other with a difference in the gain parameter. Such applications are categorized as linear applications.
2. Amplifiers that invert the input signal and amplifies are called as inverting amplifiers.
3. There are two types of OP-AMP comparator circuits, i.e., open loop comparators and closed loop comparators.

### NOTES

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### 13.4 SUMMARY

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- The applications of OP-AMP can be classified as linear applications and non-linear applications.
- In applications such as a differential amplifier, inverting and non-inverting amplifiers, instrumentation amplifiers, buffer amplifiers etc., the output voltage and input voltage are linear to each other with a difference in the gain parameter. Such applications are categorized as linear applications.
- Non-linear applications of OP-AMP include clippers, clampers, log amplifiers, antilog amplifiers, Schmitt trigger, series and shunt regulators etc.
- Amplifiers that invert the input signal and amplifies are called as inverting amplifiers.
- In non-inverting amplifiers, the input voltage is not inverted but only amplified. The gain of the amplifier gets modified and is always greater than 1.
- Differentiator can be used to perform mathematical differentiation of an input signal.
- OP-AMPs may also be used as logarithmic amplifiers. Such amplifiers are nonlinear applications of OP-AMP. They employ diode in the negative feedback circuit.
- The function of the comparator is that two input signals are compared by the OP-AMP input terminals, the output is a square pulse representing the greater voltage of the input signal.
- There are two types of OP-AMP comparator circuits, i.e., open loop comparators and closed loop comparators.

## NOTES

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### 13.5 KEY WORDS

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- **Differential amplifier:** It amplifies the difference of the two input signal voltages.
- **Integrator:** It is an electronic integration circuit which performs the mathematical operation of integration with respect to time.
- **Comparator:** It is a device that compares two voltages or currents and outputs a digital signal indicating which is larger.

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### 13.6 SELF ASSESSMENT QUESTIONS AND EXERCISES

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#### Short Answer Questions

1. Relate the input voltage and output voltage for inverting and non-inverting amplifier circuit.
2. Implement an OP-AMP circuit, that implements the function,  $V_0 = 2V_1 + 5V_2$ .
3. Draw the input-output waveform of an integrator circuit.
4. Draw the input-output waveform of a differentiator circuit.
5. What do you understand by the upper threshold voltage and lower threshold voltage?

#### Long Answer Questions

1. Explain the working of inverting amplifier with a neat diagram. Derive the output voltage expression.
2. Explain the working of a non-inverting amplifier with a neat diagram. Derive the output voltage expression.
3. Explain the working of adder circuit with neat diagram. Derive the output voltage expression.
4. Explain the working of a subtractor circuit with neat diagram. Derive the output voltage expression.
5. Explain the working of integrator circuit with neat diagram. Derive the output voltage expression.
6. Explain the working of a differentiator circuit with neat diagram. Derive the output voltage expression.
7. Explain the working of a log amplifier circuit with a neat diagram. Derive the output voltage expression.

8. Explain the working of antilog amplifier circuit with a neat diagram. Derive the output voltage expression.
9. Explain the working of Schmitt trigger with a neat diagram. Draw the input-output voltage waveform.

## NOTES

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### 13.7 FURTHER READINGS

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- Mavino, Albert, David J Bates. 2007. *Electronic Principles*. New York: McGraw Hill.
- Gayakwad, A. Ramakant. 2009. *Op-Amps and Linear Integrated Circuits*. New Jersey: Parentice Hall.
- Mehta, V. K. 2001. *Principles of Electronics*. New Delhi: S. Chand.
- Bell, David A. 2007. *Electronics Devices and Circuits*. New Jersey: Parentice Hall.

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## UNIT 14 ACTIVE FILTERS

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### NOTES

#### Structure

- 14.0 Introduction
- 14.1 Objectives
- 14.2 Filters
  - 14.2.1 Types of Filters
  - 14.2.2 Active Low Pass Filter
  - 14.2.3 First Order Active High Pass Filter
- 14.3 Answers to Check Your Progress
- 14.4 Summary
- 14.5 Key Words
- 14.6 Self Assessment Questions and Exercises
- 14.7 Further Readings

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### 14.0 INTRODUCTION

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In this unit, you will learn about the OP-AMP analog applications such as filtering of signals and wireless communications etc. OP-AMP can be used as filters. Filters may be high pass filters, low pass filters, band pass filters and band reject filters. All the filters may or may not employ OP-AMPs. Those filters that employ OP-AMP in filtering circuit are called as active filters and those filtering circuits that do not employ OP-AMP and employ only the passive circuit components are called as passive filters.

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### 14.1 OBJECTIVES

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After going through this unit, you will be able to:

- Define filters
- Discuss the various types of filters
- Explain the working and circuit diagram of filters

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### 14.2 FILTERS

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In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Ideally, a filter will not add new frequencies to the input signal, nor will it change the component frequencies of that signal, but it will change the relative amplitudes of the various frequency components and/or their phase relationships. Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject

signals in other frequency ranges. Such a filter has a gain which is dependent on signal frequency. As an example, consider a situation where a useful signal at frequency  $f_1$  has been contaminated with an unwanted signal at  $f_2$ . If the contaminated signal is passed through a circuit that has the very low gain at  $f_2$  compared to  $f_1$ , the undesired signal can be removed, and the useful signal will remain. Note that in the case of this simple example, we are not concerned with the gain of the filter at any frequency other than  $f_1$  and  $f_2$ . As long as  $f_2$  is sufficiently attenuated relative to  $f_1$ , the performance of this filter will be satisfactory. In general, however, a filter's gain may be specified at several different frequencies, or over a band of frequencies. Thus, curves of gain vs frequency and phase vs frequency are commonly used to illustrate filter characteristics, and the most widely used mathematical tools such as Fourier analysis, Laplacian domain are based in the frequency domain.

The frequency-domain behaviour of a filter is described mathematically in terms of its transfer function. This is the ratio of the Laplace transforms of its output and input signals. The voltage transfer function  $H(s)$  of a filter can, therefore, be written as:

$$T.F = H(s) = \frac{V_o(s)}{V_{in}(s)}$$

Where  $V_{in}(s)$  and  $V_o(s)$  are the input and output signal voltages and  $s$  is the complex frequency variable. Knowing the transfer function magnitude (or gain) at each frequency allows us to determine how well the filter can distinguish between signals at different frequencies. The transfer function magnitude versus frequency is called the amplitude response or sometimes, especially in audio applications, the frequency response. Similarly, the phase response of the filter gives the amount of phase shift introduced in sinusoidal signals as a function of frequency.

### Order of a Filter

The order of a filter is the highest power of the variable  $s$  in its transfer function. The order of a filter is usually equal to the total number of capacitors and inductors in the circuit. (A capacitor built by combining two or more individual capacitors is still one capacitor.) Higher-order filters will obviously be more expensive to build, since they use more components, and they will also be more complicated to design. However, higher-order filters can more effectively discriminate between signals at different frequencies. An example of a transfer function in  $S$  domain is given as

$$H(s) = \frac{S}{S^2 + S + 1}$$

## NOTES

In the frequency domain,  $S = j\omega$ , then the magnitude of the transfer function is given as,

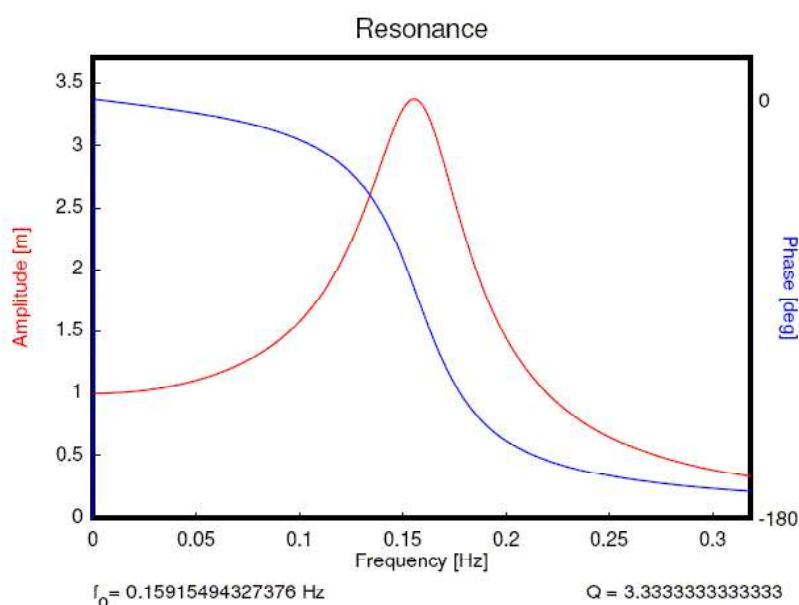
## NOTES

$$|H(j\omega)| = \left| \frac{j\omega}{-\omega^2 + j\omega + 1} \right|$$

$$\arg(H(s)) = 90^\circ - \tan^{-1} \frac{\omega^2}{1 - \omega^2}$$

### Analysis of the Effect of Frequency on Transfer Function

At very low frequencies (small values of  $s$ ), the numerator becomes very small, as do the first two terms of the denominator. Thus, as  $s$  approaches zero, the numerator approaches zero, the denominator approaches one, and  $H(s)$  approaches zero. Similarly, as the input frequency approaches infinity,  $H(s)$  also becomes progressively smaller, because the denominator increases with the square of frequency while the numerator increases linearly with frequency. Therefore,  $H(s)$  will have its maximum value at some frequency between zero and infinity and will decrease at frequencies above and below the peak.



**Fig. 14.1** Amplitude and Frequency Response of Filter Circuit

As shown in Figure 14.1, the magnitude of the transfer function has a maximum value at a certain frequency and falls off on either side of that frequency. The frequency at which the maximum amplitude is witnessed is known as centre frequency,  $f_c$ . A filter with this general shape is known as a band-pass filter because it passes signals falling within a relatively narrow band of frequencies and attenuates

signals outside of that band. The range of frequencies passed by a filter is known as the filter's pass band. In the amplitude response curve shown in Figure 14.1, there is no strict boundary that defines the pass band frequencies due to the smoothness of the amplitude response curve. Hence, from the maximum magnitude of the amplitude response curve, a gain of 3db is dropped and the corresponding frequencies on either side of the response will be specified as the limit of the pass band. The frequency corresponding to -3db drop of gain on the left side of the centre frequency is called as lower cut off frequency,  $f_l$  and the frequency on the right side of the center frequency corresponding to -3db gain drop is called as higher cut-off frequency,  $f_h$ . The center frequency is also given as,

$$f_c = \sqrt{f_l f_h}$$

### 14.2.1 Types of Filters

There are four major types of filters. They are:

- Low Pass Filter
- High Pass Filter
- Bandpass Filter
- Band Reject Filter or Band-Stop or Notch Filter

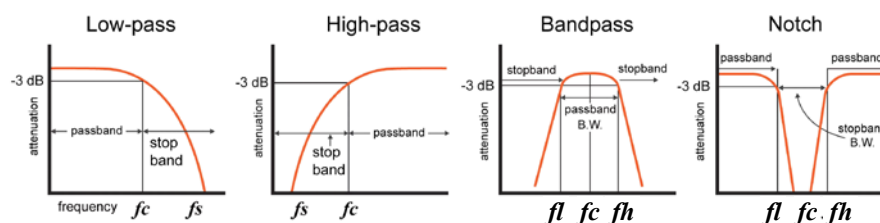
**Low Pass Filter:** filters that allow lower frequencies and reject higher frequency ranges are called as low pass filters.

**High Pass Filter:** filters that allow higher frequencies and reject lower frequency ranges are called as high pass filters.

**Bandpass Filters:** filters that allow a certain frequency ranges between the lower cut off frequency and the higher cut off frequency and reject all other frequency ranges are called bandpass filters.

**Band Reject or Band-Stop or Notch Filter:** band stop filters stops a certain range of frequencies band and allow all other frequencies are called a band reject filter.

The amplitude response of all the filter types is shown in Figure 14.2.



**Fig. 14.2** Types of Filters

## NOTES



## NOTES

## Active and Passive Filters

Passive filters are the most common type of filters that consists of passive circuit elements  $R$ ,  $L$  and  $C$ . they may exist in combinations such as  $RL$ ,  $RC$  and  $LC$  circuits. The filter circuits does not have an external power source to operate. The disadvantage with these passive circuits are in very low frequencies, the inductor gets short circuited and the capacitor gets open circuited resulting in exposing the resistor directly to the load parameters. Also, in very high frequency ranges, the passive filters become bulky. Especially, delicate design of inductors to handle high frequency components must be designed leading to high cost, bulky circuits. Hence an alternative filter design circuits using OP-AMP are considered.

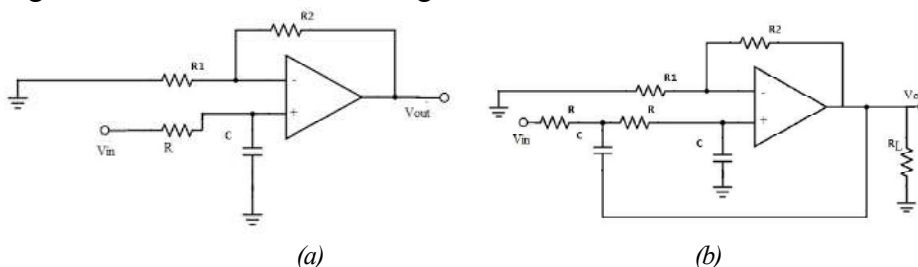
Active filter circuits are filters that employ OP-AMPs in addition to the passive circuit elements. The active filter circuits require an additional power supply to operate. The active filter circuits have the advantage of operating from very low frequency in the range of  $0\text{Hz}$  to few hundred megahertz of frequencies. Also, the advantage of OP-AMP circuits such as scalability, compact, low power functionality can be exploited when using in filter circuits. Filter circuits employing OP-AMP circuits can be fabricated into integrated circuits (ICs). Different types of active filters includes

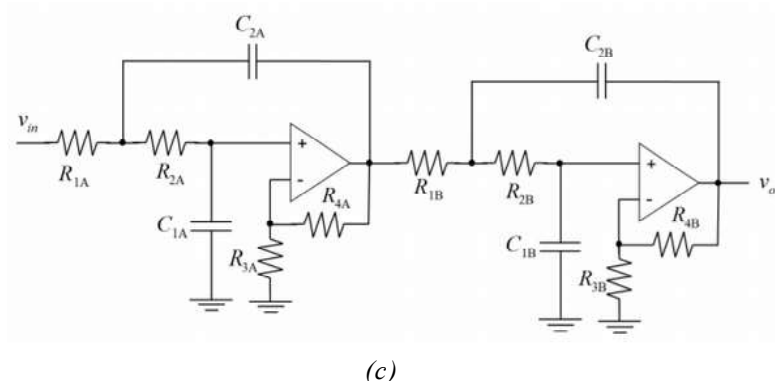
1. Butterworth Filters
2. Chebyshev Filters
3. Bessel Filters
4. Elliptical Filters

In this unit, active low pass filters, active high pass filters, active bandpass filters and active notch filters will be discussed in subsequent sections.

## 14.2.2 Active Low Pass Filter

As discussed earlier, the order of the filter circuit is determined by the number of reactive elements such as a capacitor,  $C$  and inductor,  $L$  in the circuit. Active filters on the other hand, unlike passive filters, do not use inductors for filtering purpose. The advantage of OP-AMP will be defeated if, inductors are used in filtering purposes. In this chapter, first order filters will be focused for discussion. Few higher order filters are shown in Figure 14.3.





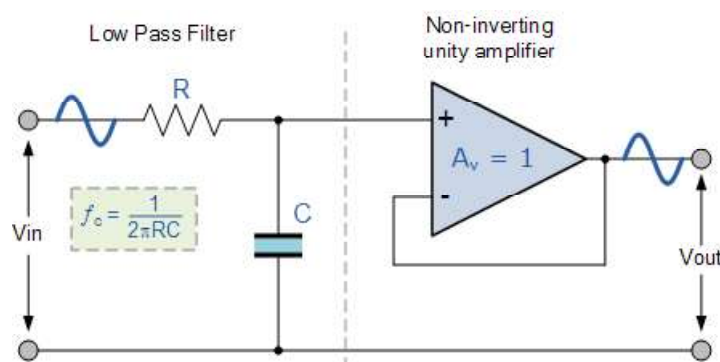
(c)

**Fig. 14.3** Types of Low Pass filters (a) First Order, (b) Second Order, (c) Third Order

As shown in Figure 14.3 (a), there is one reactive component and hence the circuit is a first order low pass filter. Similarly, based on the number of capacitor elements in Figures 14.3 (b) and 14.3 (c) are second order and third order low pass filters respectively.

### Description of First Order Low Pass Filter

First order low pass filter is similar to the RC network filter. The only difference is that the active filters employ OP-AMP for amplification and gain control through the feedback network of OP-AMP. Further, the low pass filter may further depend on whether the signal input is being fed to inverting or non-inverting terminals. Consider a unity gain first order active low pass filter as shown in Figure 14.4.



**Fig. 14.4** Active First Order Low Pass Filter (Unity Gain)

This first-order low pass active filter consists simply of a passive RC filter stage providing a low-frequency path to the input of a non-inverting operational amplifier. The amplifier is configured as a voltage-follower (Buffer)/unity gain amplifier giving it a DC gain of one,  $A_v = +1$  or unity gain as opposed to the previous passive RC filter which has a DC gain of less than unity.

The advantage of this configuration is that the OP-AMPs high input impedance prevents excessive loading on the output of the filter while its low

## NOTES

## NOTES

output impedance prevents the filter's cut-off frequency point from being affected by changes in the impedance of the load.

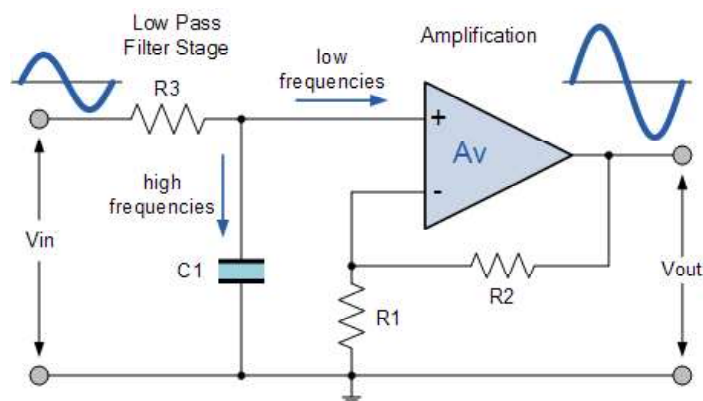
While this configuration provides good stability to the filter, its main disadvantage is that it has no voltage gain above one. However, although the voltage gain is unity the power gain is very high as its output impedance is much lower than its input impedance. If a voltage gain greater than one is required we can replace the unity gain feedback circuit with a potential divider circuit in the feedback section. The feedback resistor can be tuned to obtain the desired gain.

**Active Low Pass Filter with Gain Control**

The frequency response of the circuit will be the same as that for the passive RC filter, except that the amplitude of the output is increased by the passband gain,  $A_F$  of the amplifier. For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor ( $R_2$ ) divided by its corresponding input resistor ( $R_1$ ) value and is given as:

$$Gain = \left( 1 + \frac{R_2}{R_1} \right)$$

The active low pass filter with gain control is shown in Figure 14.5.



**Fig. 14.5** Active First Order Low Pass Filter (Gain Control)

Therefore, the gain of an active low pass filter as a function of frequency will be:

The gain of a first-order low pass filter is given as:

$$\text{Voltage Gain, } A_v = \frac{V_0}{V_{in}} = \frac{A_F}{\sqrt{1 + \left( \frac{f}{f_c} \right)^2}}$$

Where:

- $A_F$  = The passband gain of the filter,  $(1 + R_2 / R_1)$
- $f$  = The frequency of the input signal in Hertz, (Hz)
- $f_c$  = The cut-off frequency in Hertz, (Hz)

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies,  $f < f_c \Rightarrow A_v \approx A_F$
2. At the cut-off frequency,  $f = f_c \Rightarrow A_v = \frac{A_F}{\sqrt{2}} = 0.707 A_F$
3. At very high frequencies,  $f > f_c \Rightarrow A_v < A_F$

Thus, the **Active Low Pass Filter** has a constant gain  $A_F$  from 0 Hz to the high-frequency cut-off point,  $f_c$ . At  $f_c$ , the gain is  $0.707 A_F$ , and after  $f_c$ , it decreases at a constant rate as the frequency increases. That is when the frequency is increased tenfold (one decade), the voltage gain is divided by 10.

In other words, the gain decreases 20dB ( $= 20 \cdot \log(10)$ ) each time the frequency is increased by 10. When dealing with filter circuits the magnitude of the passband gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

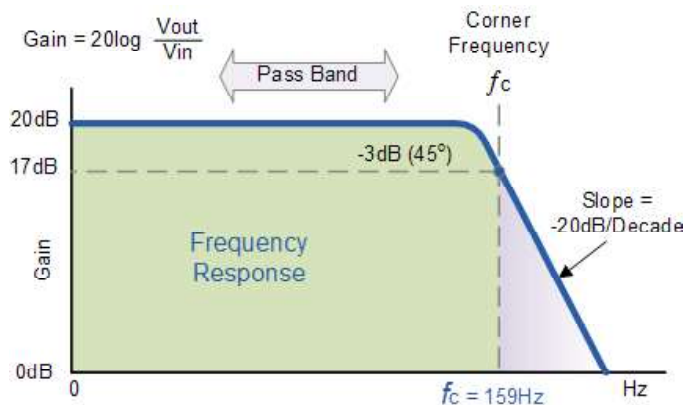
#### The Magnitude of Voltage Gain in (dB)

$$A_v = 20 \log_{10} \left( \frac{V_o}{V_{in}} \right)$$

When the gain is at  $0.707 A_F$ , then

$$A_v = 20 \log_{10} \left( \frac{0.707 V_o}{V_{in}} \right) = -3 \text{ dB}$$

The frequency response curve for an active low pass filter is shown in Figure 14.6.

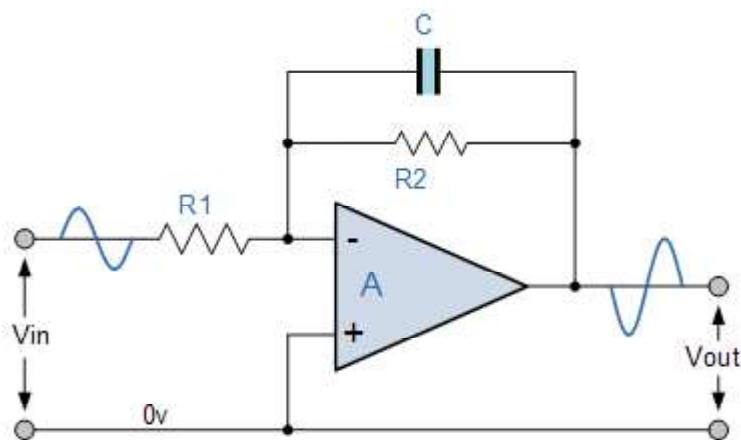


**Fig. 14.6** Frequency Response Curve

#### NOTES

The above discussion pertains to non-inverting amplifier filter. The equivalent circuit for inverting amplifier filter circuit is shown in Figure 14.7.

## NOTES

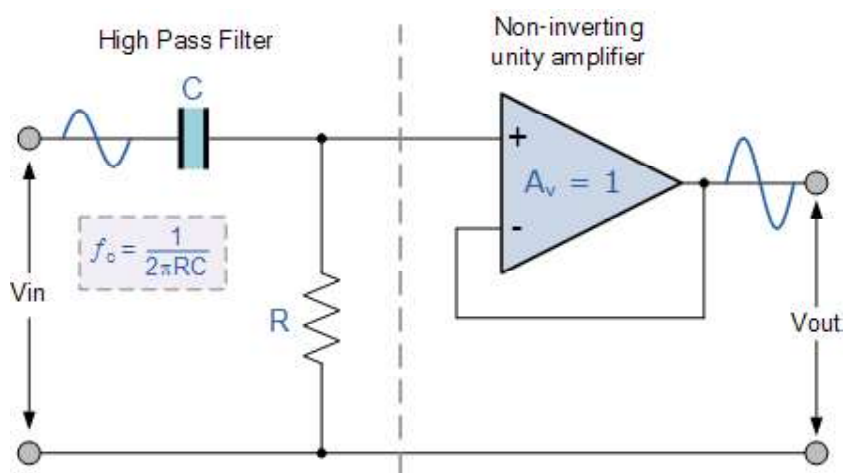


**Fig. 14.7** Inverting Amplifier Low Pass Filter Circuit

## Applications

Applications of **Active Low Pass Filters** are in audio amplifiers, equalizers or speaker systems to direct the lower frequency bass signals to the larger bass speakers or to reduce any high-frequency noise or “hiss” type distortion. When used like this in audio applications the active low pass filter is sometimes called a “Bass Boost” filter.

### 14.2.3 First Order Active High Pass Filter

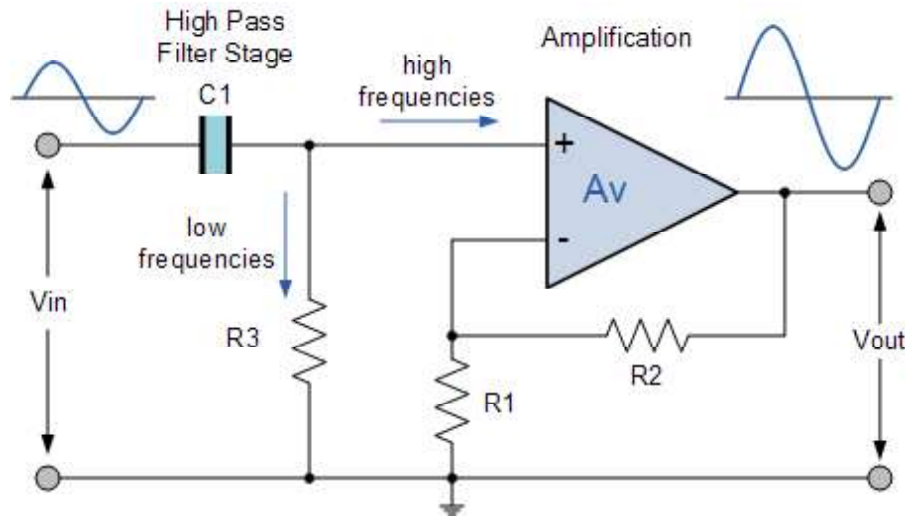


**Fig. 14.8** Non-Inverting OP-AMP First Order High Pass Filter

A first-order **active high pass filter** as its name implies attenuates low frequencies and passes high-frequency signals. It consists simply of a passive filter section followed by a non-inverting operational amplifier. The frequency response of the circuit is the same as that of the passive filter, except that the amplitude of the signal is increased by the gain of the amplifier. A unity gain active high pass filter

is shown in Figure 14.8. When the unity feedback part is replaced with a combination of potential divider resistors as shown in Figure 14.9, active high pass filter with amplification is obtained.

### Active High Pass Filter with Amplification



**Fig. 14.9** Active High Pass Filter with Gain

For a non-inverting amplifier circuit, the magnitude of the voltage gain for the filter is given as a function of the feedback resistor ( $R_2$ ) divided by its corresponding input resistor ( $R_1$ ) value and is given as:

$$\text{The gain for an Active High Pass Filter, } A_v = \frac{V_o}{V_{in}} = \frac{A_{ol} \left( \frac{f}{f_c} \right)}{\sqrt{1 + \left( \frac{f}{f_c} \right)^2}}$$

Where:

- $A_F$  = The Pass band Gain of the filter,  $(1 + R_2 / R_1)$
- $f$  = The Frequency of the Input Signal in Hertz, (Hz)
- $f_c$  = The Cut-off Frequency in Hertz, (Hz)

similar to the low pass filter, the operation of a high pass active filter can be verified from the frequency gain equation above as:

1. At very low frequencies,  $f < f_c \Rightarrow A_v < A_F$
2. At the cut-off frequency,  $f = f_c \Rightarrow A_v = \frac{A_F}{\sqrt{2}} = 0.707 A_F$
3. At very high frequencies,  $f > f_c \Rightarrow A_v \approx A_F$

### NOTES

**NOTES**

Then, the **Active High Pass Filter** has a gain  $A_F$  that increases from 0Hz to the low-frequency cut-off point,  $f_c$  at 20dB/decade as the frequency increases. At  $f_c$ , the gain is  $0.707 \times A_F$ , and after  $f_c$  all frequencies are pass band frequencies so the filter has a constant gain  $A_F$  with the highest frequency being determined by the closed loop bandwidth of the OP-AMP.

When dealing with filter circuits the magnitude of the passband gain of the circuit is generally expressed in *decibels* or *dB* as a function of the voltage gain, and this is defined as:

**The magnitude of Voltage Gain in (dB)**

$$A_v = 20 \log_{10} \left( \frac{V_o}{V_{in}} \right)$$

When the gain is at  $0.707 A_F$ , then

$$A_v = 20 \log_{10} \left( \frac{0.707 V_o}{V_{in}} \right) = -3 \text{ dB}$$

The frequency response curve for an active low pass filter is shown in Figure 14.11.

For a first-order filter the frequency response curve of the filter increases by 20dB/decade or 6dB/octave up to the determined cut-off frequency point which is always at -3dB below the maximum gain value. As with the previous filter circuits, the center frequency (  $f_c$  ) can be found by using the same formula:

$$f_c = \frac{1}{2\pi RC} \text{ Hz}$$

The corresponding phase angle or phase shift of the output signal is the same as that given for the passive RC filter and leads that of the input signal. It is equal to  $+45^\circ$  at the center frequency  $f_c$  value and is given as:

$$\text{Phase Shift, } \phi = \tan^{-1} \left( \frac{1}{2\pi RC} \right)$$

A simple first-order active high pass filter can also be made using an inverting operational amplifier configuration as well, and an example of this circuit design is given along with its corresponding frequency response curve. A gain of 40dB has been assumed for the circuit.

## Inverting Operational Amplifier Circuit

Active Filters

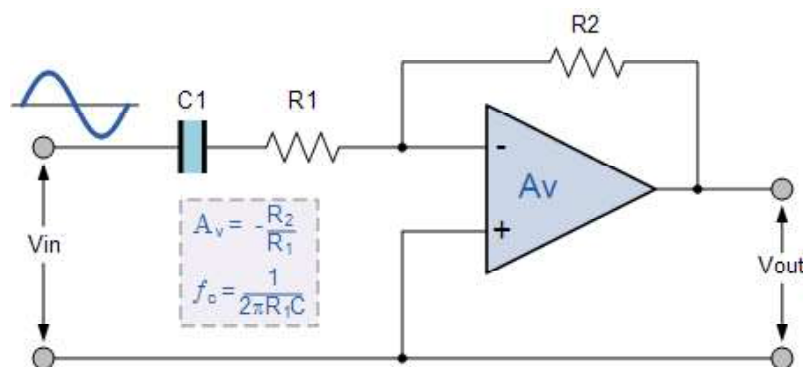


Fig. 14.10 Inverting Amplifier First Order Low Pass Filter

## Frequency Response Curve

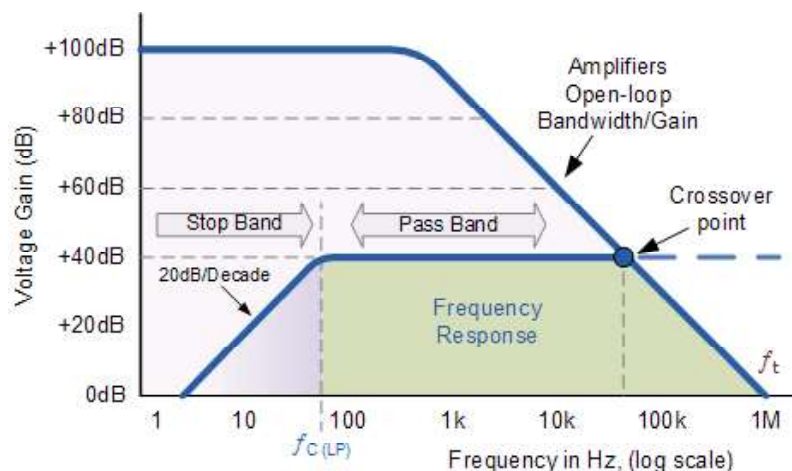


Fig. 14.11 Frequency Response of First Order High Pass Filter

### 14.2.4 Active Bandpass Filter

For a low pass filter, this passband starts from 0Hz or DC and continues up to the specified cut-off frequency point at -3dB down from the maximum passband gain. Equally, for a high pass filter the passband starts from this -3dB cut-off frequency and continues up to infinity or the maximum open loop gain for an active filter.

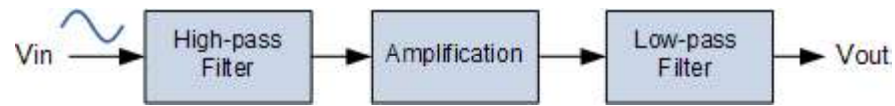
However, the **Active Band Pass Filter** is slightly different in that it is a frequency selective filter circuit used in electronic systems to separate a signal at one particular frequency, or a range of signals that lie within a certain “band” of frequencies from signals at all other frequencies. This band or range of frequencies is set between two cut-off or corner frequency points labeled the “lower cutoff frequency” ( $f_L$ ) and the “higher cutoff frequency” ( $f_H$ ) while attenuating any signals outside of these two points.

## NOTES



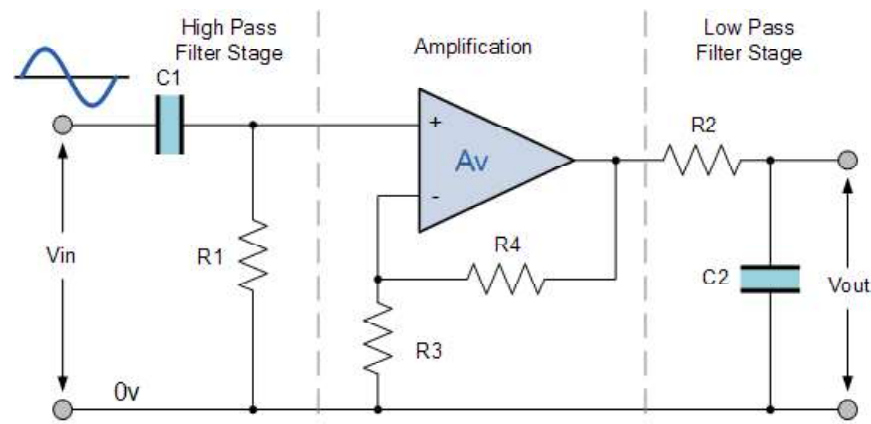
Simple active band pass filter can be easily made by cascading together a single Low Pass Filter with a single High Pass Filter as shown in Figure 14.12.

## NOTES



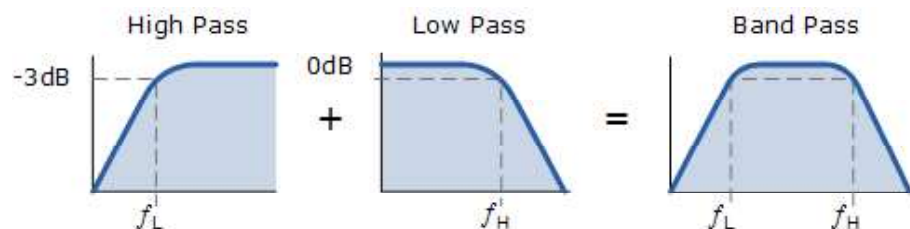
**Fig. 14.12** Block Diagram of Bandpass Filter

The cutoff frequency of the low pass filter (LPF) is higher than the cut-off frequency of the high pass filter (HPF) and the difference between the frequencies at the -3dB point will determine the “bandwidth” of the bandpass filter while attenuating any signals outside of these points. One way of making a very simple **active band pass filter** is to connect the basic passive high and low pass filters that were discussed in earlier sections to an amplifying OP-AMP circuit as shown in Figure 14.13.



**Fig. 14.13** Active Bandpass Filter Made from the Low Pass and High Pass Filter

This cascading together of the individual low and high pass passive filters produces a low “Q-factor” type filter circuit which has a wide passband. The first stage of the filter will be the high pass stage that uses the capacitor to block any DC biasing from the source. This design has the advantage of producing a relatively flat asymmetrical passband frequency response with one half representing the low pass response and the other half representing high pass response as shown in Figure 14.14.

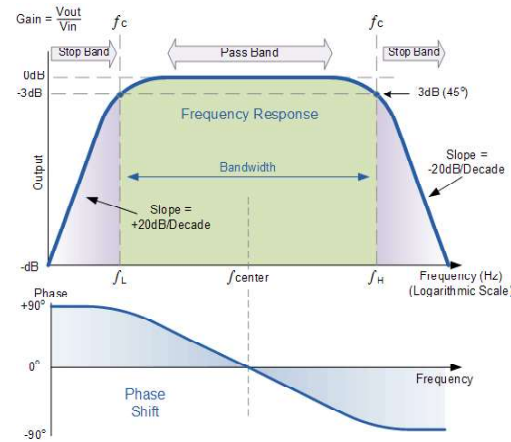


**Fig. 14.14** Bandpass Frequency Response from the Low Pass and High Pass Frequency Response

## Active Band Pass Frequency Response

The higher cut-off frequency ( $f_H$ ), as well as the lower cut-off frequency ( $f_L$ ), are calculated the same as before in the standard first-order low and high pass filter circuits. Obviously, a reasonable separation is required between the two cut-off points to prevent any interaction between the low pass and high pass stages. The amplifier also provides isolation between the two stages and defines the overall voltage gain of the circuit.

## NOTES



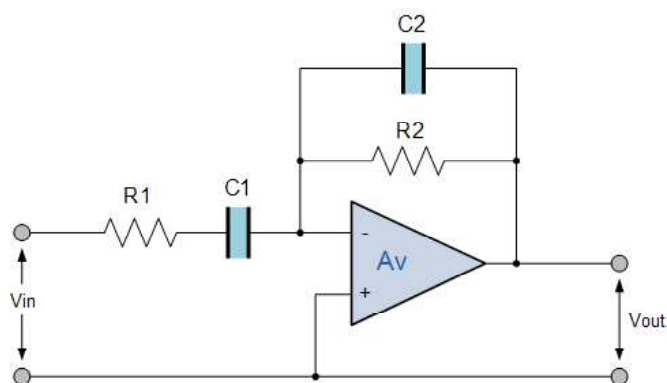
**Fig. 14.15** Normalized Amplitude and Phase Response to Frequency for a Bandpass Filter

The bandwidth of the filter is, therefore, the difference between these upper and lower -3dB points. For example, suppose we have a bandpass filter whose -3dB cut-off points are set at 200Hz and 600Hz. Then the bandwidth of the filter would be given as Bandwidth (BW) = 600 – 200 = 400Hz.

The normalized frequency response and phase shift for an active band pass filter will be as shown in Figure 14.15. While the given passive tuned filter circuit will work as a bandpass filter, the passband (bandwidth) can be quite wide and this may be a problem if we want to isolate a small band of frequencies. The active bandpass filter can also be made using an inverting operational amplifier.

On detailed analysis of the equivalent resistance and equivalent capacitance in the output circuit and in the feedback circuit, the bandwidth of the band pass filter can be fine-tuned to provide a much better frequency response. Hence by rearranging the positions of the resistors and capacitors within the filter, we can produce a much better filter circuit as shown in Figure 14.16. For an active bandpass filter, the lower cut-off -3dB point is given by  $f_{C1}$  while the upper cut-off -3dB point is given by  $f_{C2}$ .

## NOTES



**Fig. 14.16** Inverting Band Pass Filter Circuit

The voltage gain for the above circuit is given as

$$\text{Voltage Gain, } A_v = -\frac{R_2}{R_1} f_{c1} = \frac{1}{2\pi R_1 C_1} f_{c2} = \frac{1}{2\pi R_2 C_2}$$

This type of bandpass filter is designed to have a much narrower passband. The center frequency and bandwidth of the filter are related to the values of  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$ . The output of the filter is again taken from the output of the OP-AMP.

#### Check Your Progress

1. What is a filter?
2. How will you find the order of a filter?
3. What are the different types of filters?
4. Write the applications of active low pass filters.

### 14.3 ANSWERS TO CHECK YOUR PROGRESS

1. A filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency.
2. The order of a filter is the highest power of the variable  $s$  in its transfer function. The order of a filter is usually equal to the total number of capacitors and inductors in the circuit.
3. There are four major types of filters i.e. low pass filter, high pass filter, band pass filter and band reject filter or notch filter.
4. Applications of active low pass filters are in audio amplifiers, equalizers or speaker systems to direct the lower frequency bass signals to the larger bass speakers or to reduce any high-frequency noise or “hiss” type distortion.

## 14.4 SUMMARY

- A filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency.
- Filters are often used in electronic systems to emphasize signals in certain frequency ranges and reject signals in other frequency ranges.
- The frequency-domain behaviour of a filter is described mathematically in terms of its transfer function. This is the ratio of the Laplace transforms of its output and input signals.
- The order of a filter is the highest power of the variable  $s$  in its transfer function. The order of a filter is usually equal to the total number of capacitors and inductors in the circuit.
- There are four major types of filters, i.e., low pass filter, high pass filter, band pass filter and band reject filter or notch filter.
- Passive filters are the most common type of filters that consists of passive circuit elements  $R$ ,  $L$  and  $C$ .
- Active filter circuits are filters that employ OP-AMPs in addition to the passive circuit elements.
- Applications of active low pass filters are in audio amplifiers, equalizers or speaker systems to direct the lower frequency bass signals to the larger bass speakers or to reduce any high-frequency noise or “hiss” type distortion.
- Active band pass filter is slightly different in that it is a frequency selective filter circuit used in electronic systems to separate a signal at one particular frequency, or a range of signals that lie within a certain “band” of frequencies from signals at all other frequencies.

## NOTES

## 14.5 KEY WORDS

- **Passive filter:** A filter which uses passive component like inductor, capacitor, resistance, etc. for its construction is called passive filters.
- **Active filter:** An active filter additionally uses an amplifier to provide voltage amplification and signal isolation or buffering.
- **Low-pass filter** A filter that provides a constant output from dc up to a cut-off frequency and then passes no signal above that frequency is called an ideal low-pass filter.
- **High-pass filter:** A filter that provides or passes signals above a cut-off frequency is a high-pass filter.

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## 14.6 SELF ASSESSMENT QUESTIONS AND EXERCISES

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### NOTES

#### Short Answer Questions

1. What is bandwidth?
2. Define lower cut-off frequency.
3. Define higher cut-off frequency.
4. Draw the block diagram of the band pass filter.
5. What do you understand by center frequency?
6. Compare the active filter circuits and passive filter circuits.
7. Compare the various filter circuits.

#### Long Answer Questions

1. Describe in detail the working of low pass filter with relevant diagrams and frequency response plot.
2. Describe in detail the working of high pass filter with relevant diagrams and frequency response plot.
3. Describe in detail the working of a bandpass filter with relevant diagrams and frequency response plot.
4. What is the importance of the feedback network in filter circuits?

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## 14.7 FURTHER READINGS

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